

Figure 1. Physical Photos of ATDC2934

ORDERING GUIDE

Online Stores		Commission Fee	Unit Price (June 2024)	Buy Now
AS	shop.analogtechnologies **Our own online store**	Zero sale commission	$0.66/PCs (≥100PCs)	*
SZ	SMTZone **Our own online store**	Zero sale commission	$0.66/PCs (≥100PCs)	*
K	Digikey	≈500% sale commission	$3.94/PCs (≥100PCs)	*

Table 1. ATDC2934

Parameter	ATDC2934
Input Voltage	5V~42V
Output Voltage	0.8V to 20V
Output Current	600mA
Switching Frequency	1.2MHz
Efficiency	≥95%@V_{IN} = 12V & I_{IN} = 400mA

FEATURES

- Wide Input Voltage Range: 5V to 42V
- Adjustable Output Voltage: 0.8V to 0.9V_{IN}
- Output Current: Up to 600mA
- Ultra Low Shutdown Current: < 0.6μA
- 1.2MHz Switching Frequency
- High Efficiency Up to 95%@V_{IN} = 12V & I_{IN} = 400mA
- Internal Compensation and Soft-Start

APPLICATIONS

- Automotive Systems
- Automotive Battery Regulation
- Standby Power for Portable Products
- Distributed Supply Regulation
- Industrial Control Supplies
- FPGA, DSP, ASIC Power Supplies

DESCRIPTION

The ATDC2934 is a current mode PWM step-down DC/DC converter with a 0.9Ω Internal Power MOSFET. With its wide input range of 5V to 42V, the ATDC2934 can regulate a wide variety of power sources. The output voltage of the ATDC2934 can be down to 0.8V, and the output current can be up to 600mA. The current mode control provides fast transient response and cycle-by-cycle over current protection. The shutdown current is 0.6μA typical. Adjustable soft start prevents inrush current at turn on. The ATDC2934 features an over temperature shutdown protection.

The 1.2 MHz operating frequency allows small inductor and ceramic capacitors to be used, providing a compact solution. Current mode control provides fast and stable line and load transient performance.

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The ATDC2934 allows the use of small external components while still being able to have low output voltage ripple. A soft-start function can be implemented using the enable pin and by connecting an external RC circuit allowing the user to tailor the soft-start time to a specific application.

The ATDC2934 is in a thermally enhanced SOT-23-6 package which comes with a heat sink solder pad underneath, and it is RoHS compliant and 100% lead (Pb) free.

PIN CONFIGURATION

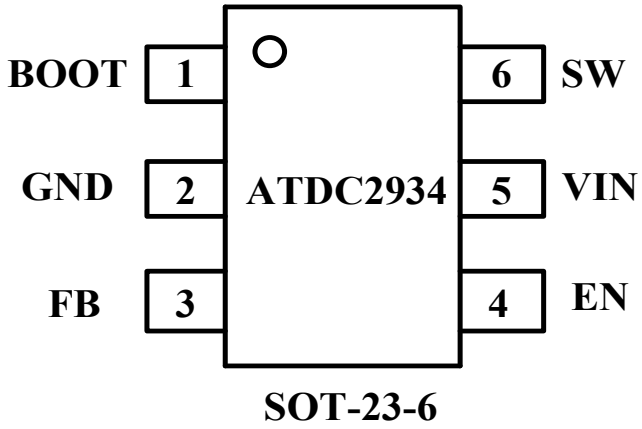


Figure 3. Pin Configuration

APPLICATION CIRCUIT

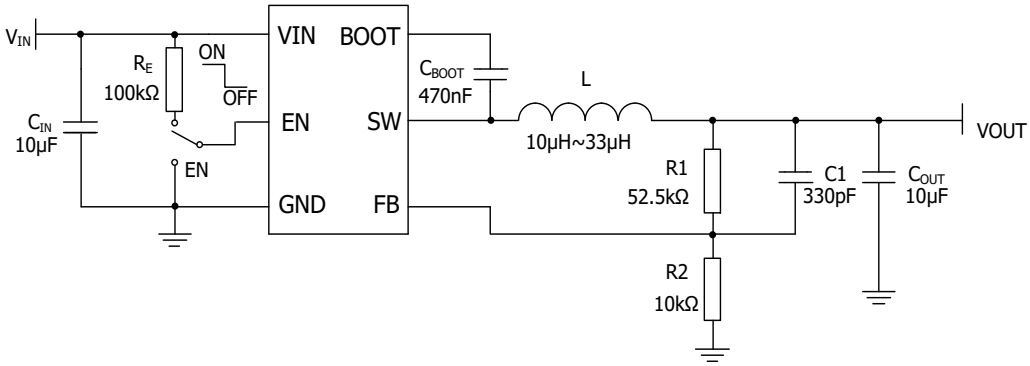


Figure 4. Typical Application Circuit

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PIN FUNCTIONS

Table 2. Pin Names, Types and Descriptions.

NO.	NAME	DESCRIPTION
1	BOOST	Bootstrap pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. Place a 0.47μF boost capacitor (C_{BOOT}) as close as possible to the IC between this pin and SW pin. Do not place a resistor in series with this pin.
2	GND	Ground. Connect all the input and output capacitors to GND.
3	FB	Feedback pin for programming the output voltage. The ATDC2934 regulates the FB pin to 0.8V. Connect the feedback resistor divider tap to this pin. If the FB voltage exceeds 110% of 0.8V, over-voltage protection (OVP) will stop all PWM switching.
4	EN	Enable pin should not be left open and it should not be driven above VIN + 0.3V. Device will operate when the EN pin is high and shut down when the EN pin is low. EN can be tied to VIN pin via a resistor if the shutdown feature is not required or to a logic input for controlling shutdown.
5	VIN	The VIN pin supplies current to the ATDC2934's internal regulator and to the internal power switch. This voltage is monitored by a UVLO lockout comparator. VIN is also connected to the drain of the converter top switch. Due to power switching, this pin has high di/dt transition edges and must be decoupled to the GND by input capacitors as close as possible to the GND pin to minimize the parasitic inductances.
6	SW	Switching node pin is the output of the internal power converter and should be connect to the output inductor. Bootstrap capacitor also connects to this pin. This node should be kept small on the PCB to minimize capacitive coupling, noise coupling and radiation.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Input Voltage V_{IN}	5V ~ 42V
BOOST Pin Above SW Pin	-0.3V to 5.5V
EN Pin	-0.3V to V_{IN}+0.3V
FB Voltage	-0.3V to 5.5V
SW Voltage	-0.3V to V_{IN}+0.3V
Operating Temperature Range	−40°C ~ 85°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C ~ 150°C
Lead Temperature (Soldering, 10 sec)	260°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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ELECTRICAL CHARACTERISTICS

Table 3. T_A = 25°C. V_{IN} = 12V, unless otherwise noted.

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit/Note
Input Voltage		V_{IN}	−40°C ≤ T_A ≤ 125°C	5	–	42	V
Under-Voltage Lockout Threshold		V_{UVLO}		4.45	4.7	4.95	mA
Under-Voltage Lockout Threshold Hysteresis		V_{UVLO_HYS}		–	370	1.2	mV
Switching Frequency		f_{SW}		0.85	1.2	1.5	MHZ
Switch Leakage Current		I_{SW_H}	V_{SW} = 42V		0.1	1	μA
		I_{SW_L}	V_{SW} = 0V		0.1	1	μA
Feedback Reference Voltage		V_{FB}	V_{IN} = 6V	0.777	0.800	0.823	V
Feedback Pin Input Current		I_{FB}	V_{FB} = 1V		0.1	1	μA
V_{IN} Quiescent Current	Shutdown	I_Q	V_{EN} = 0V		150		°C
	Sleep Mode		V_{EN} = 2V, Not Switching, V_{IN} ≤ 36V		125		°C
Minimum High-side Switch On Time		t_{ON_MIN}	I_{LOAD} = 600mA		100		ns
Minimum High-side Switch Off-Time		t_{OFF_MIN}			100		ns
Top Power NMOS Current Limit		I_{LIM}	T_J = +25°C	0.9	1.2	1.5	A
Top Power NMOS On-Resistance		R_{DSON}	I_{LOAD} = 0.1A		700		mΩ
Bottom Power NMOS On-Resistance			I_{LOAD} = 0.1A		300		mΩ
EN Input High Voltage		V_{IH}		1.2			V
EN Input Low Voltage		V_{IL}				0.5	V
EN Threshold, Hysteresis		V_{EN_HYS}			120		mV
Enable Leakage Current		I_{EN}	V_{EN} = 5V		0.1	1	μA
Output Over-Voltage Threshold		V_{OUT_OV}	OVP Rising	0.84	0.89	0.95	V
			OVP Falling	0.85	0.85	0.90	V
Thermal Shutdown		T_{SHDN}			150		°C
Thermal Shutdown Hysteresis		T_{HYS}			20		°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ATDC2934 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The ATDC2934 specification is guaranteed over the –40°C to 125°C temperature range.

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TYPICAL PERFORMANCE CHARACTERISTICS

T_A=25°C, V_{IN}=18V, L=22µH and C_{OUT}=10µF, unless otherwise noted.

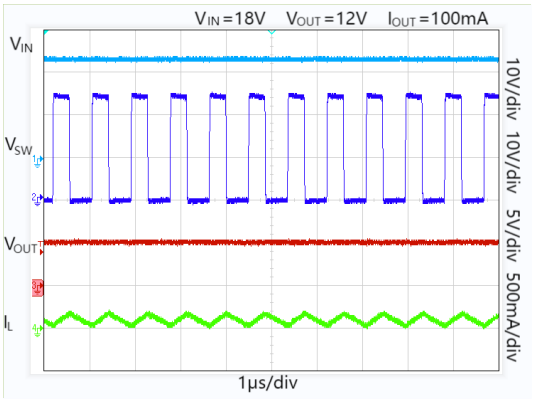


Figure 5. Steady State

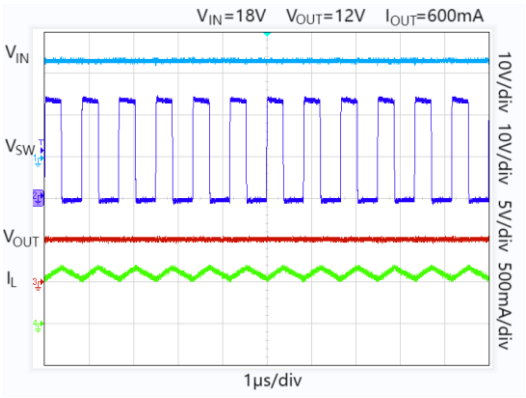


Figure 6. Steady State

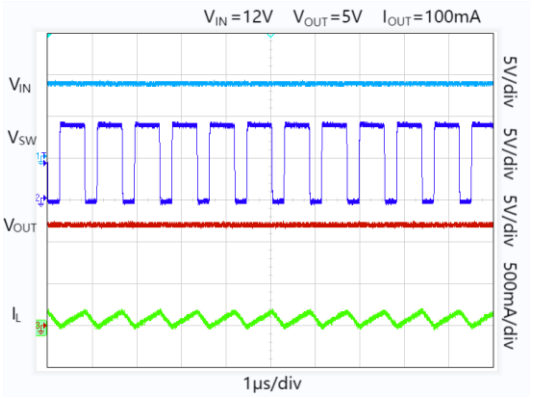


Figure 7. Steady State

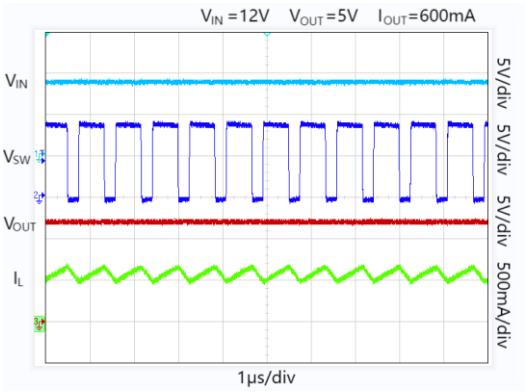


Figure 8. Steady State

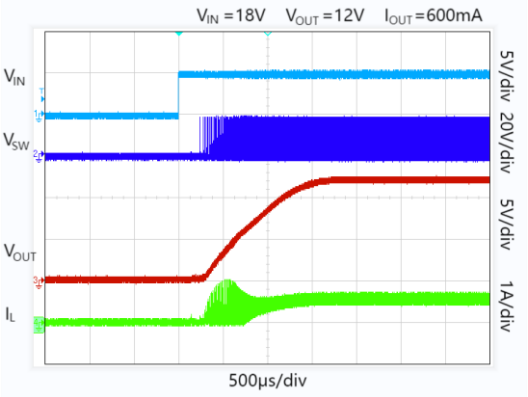


Figure 9. Power-Up

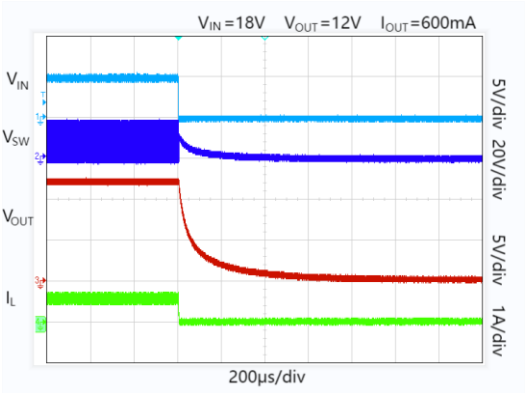


Figure 10. Power-Down

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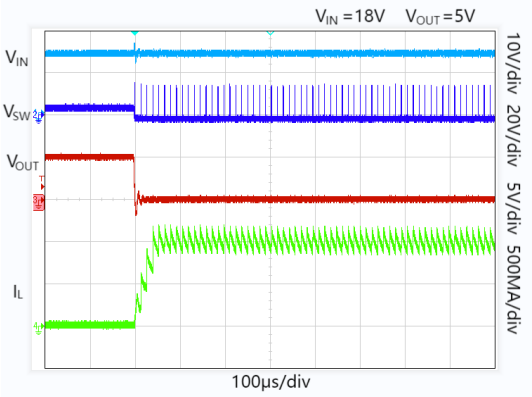


Figure 11. Short-Circuit Entry

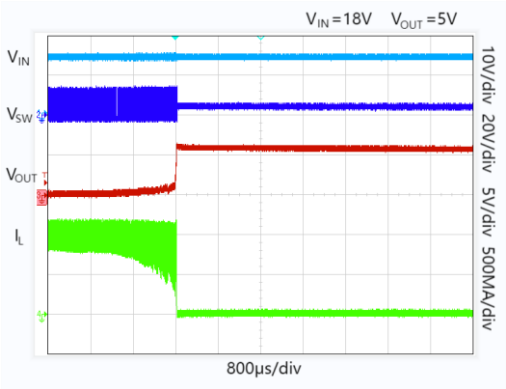


Figure 12. Short-Circuit Recovery

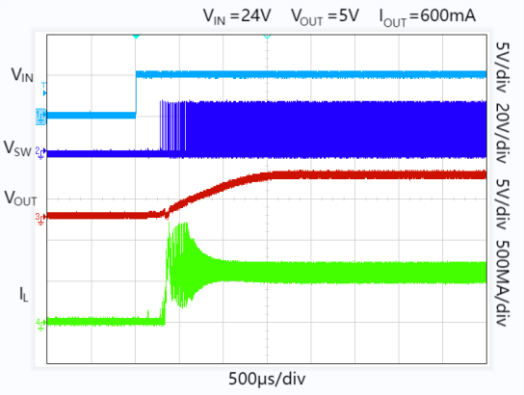


Figure 13. Power-Up

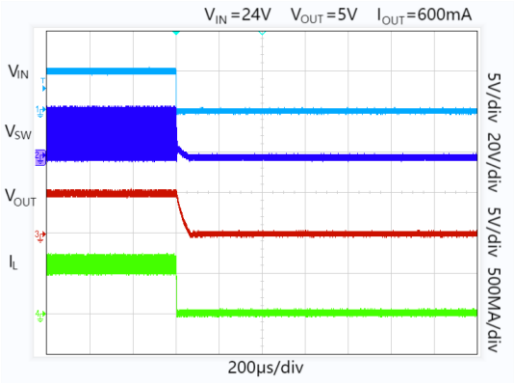


Figure 14. Power-Down

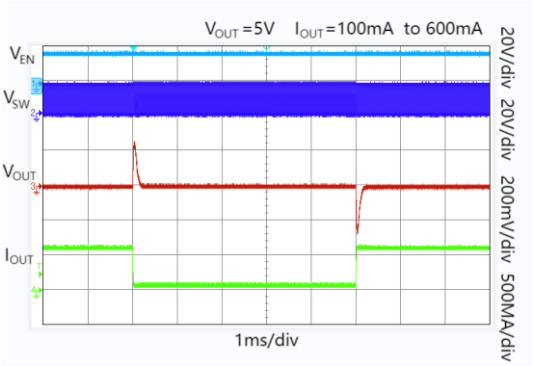


Figure 15. Load Transient Response

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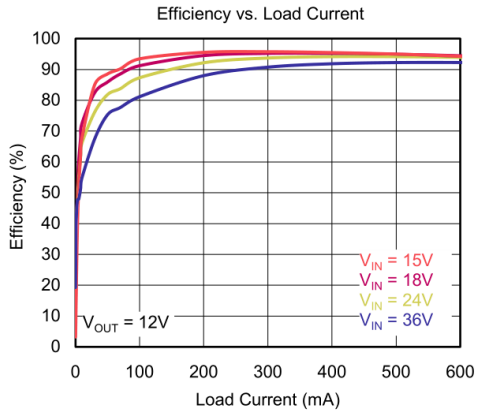


Figure 16. Efficiency vs. Load Current @ V_{OUT}=12V

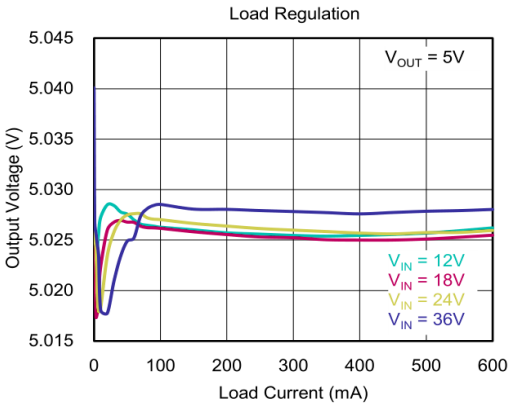


Figure 19. Load Regulation

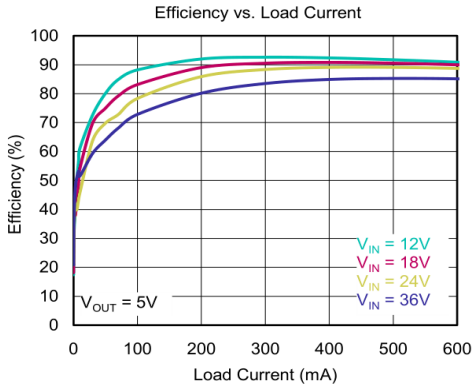


Figure 17. Efficiency vs. Load Current @ V_{OUT}=5V

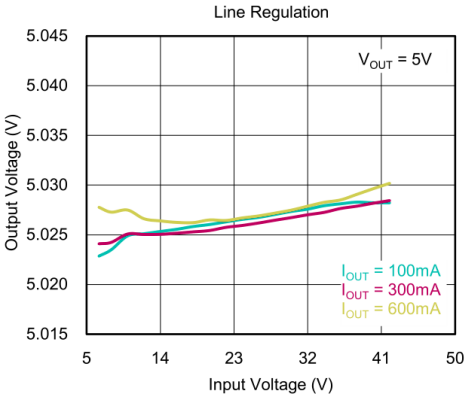


Figure 20. Line Regulation

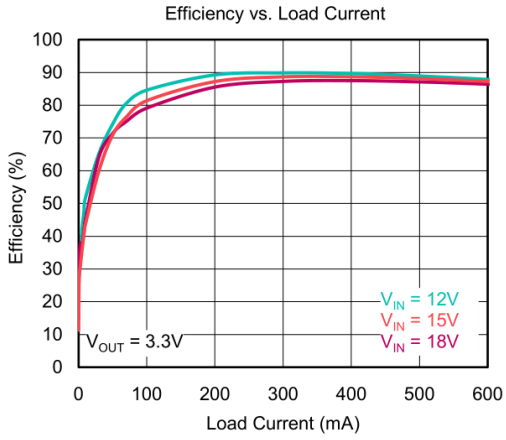


Figure 18. Efficiency vs. Load Current @ V_{OUT}=3.3V

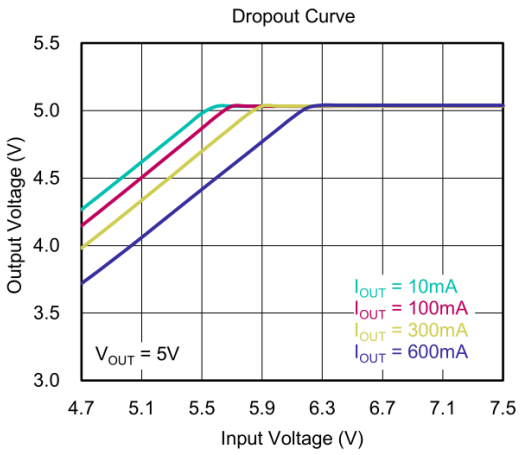


Figure 21. Dropout Curve

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FUNCTIONAL BLOCK DIAGRAM

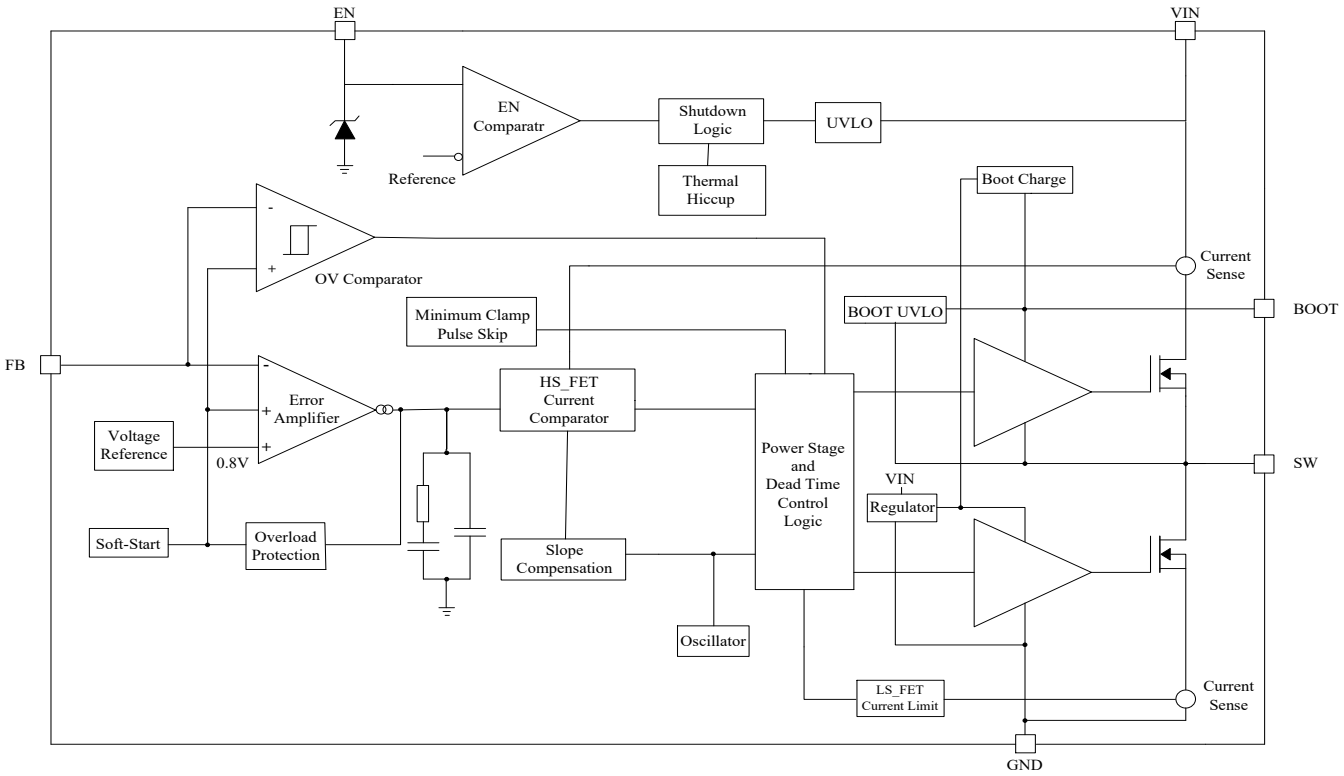


Figure 22. Block Diagram

APPLICATION INFOR MATION

Overview

The ATDC2934 is an internally compensated wide input range current mode controlled synchronous step-down converter. It is designed for high reliability and is particularly suitable for power conditioning from unregulated sources or battery-powered applications that need low sleep/shutdown currents. It also features a power-save mode in which operating frequency is adaptively reduced under light load conditions to reduce switching and gate losses and keep high efficiency. At no load and with switching stopped, the total operating current is approximately 14μA. If the device is disabled, the total consumption is typically 0.6μA.

Figure 22 shows the simplified block diagram of the ATDC2934. The two integrated MOSFET switches of the power stage are both over-current protected and can provide up to 600mA of continuous current for the load. Current limiting of the switches also prevents inductor current runaway. The converter switches are optimized for high efficiency at low duty cycle.

At the beginning of each switching cycle, the high-side switch is turned on. This is the time that feedback voltage (V_{FB}) is below the reference voltage (V_{REF}) and power must be delivered to the output. After the on-period, the high-side switch is turned off and the low-side switch is turned on until the end of switching cycle. For reliable operation and preventing shoot through, a short dead time is always inserted between gate pulses of the converter complimentary switches. During dead time, both switch gates are kept off.

The device is designed for safe monotonic start-up even if the output is pre-biased.

If the junction temperature exceeds a maximum

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threshold (T_{SHDN}, typically +150°C), thermal shutdown. protection will happen and switching will stop. The device will automatically recover with soft-start when the junction temperature drops back well below the trip point. This hysteresis is typically 20°C.

The ATDC2934 has current limit on both the high-side and low-side MOSFET switches. When current limit is activated frequency fold-back is also activated. This occurs in the case of output overload or short circuit. Note that ATDC2934 will continue to provide its maximum output current and will not shut down or hiccup. In such a case, the junction temperature may rise rapidly and trigger thermal shutdown.

During initial power-up of the device (soft-start), current limit and frequency fold-back are activated to prevent inductor current runaway while the output capacitor is charging to the desired V_{OUT}.

Peak-Current Mode (PWM Control)

Figure 22 shows the functional block diagram and Figure 23 shows the switching node operating waveforms of the ATDC2934. Switching node voltage is generated by controlling the duty cycles of the complementary high-side and low-side switches. The duty cycle of the high-side switch is used as control parameter of the buck converter to regulate output voltage and is defined as: $D = t_{ON}/t_{SW}$, where t_{ON} is the high-side switch on-time and t_{SW} is the switching period. During high-side switch on-time, the SW pin voltage swings up to approximately V_{IN} , and the inductor current, I_L , linearly rises with a slope of $(V_{IN}-V_{OUT})/L$. When control logic turns off the high-side switch, the low-side switch will turn on after a short dead time. During off-time, inductor current discharges through the low-side switch with a slope of $(-V_{OUT}/L)$. In ideal case, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D=V_{OUT}/V_{IN}$.

The ATDC2934 employs fixed-frequency peak-current mode control in continuous conduction mode (when inductor minimum current is above zero). In light load conditions (when the inductor current reaches zero) the ATDC2934 will enter discontinuous conduction mode and the control mode will change to shift frequency, peak-current mode to reduce the switching frequency and the associated switching and gate driving losses (power-save mode).

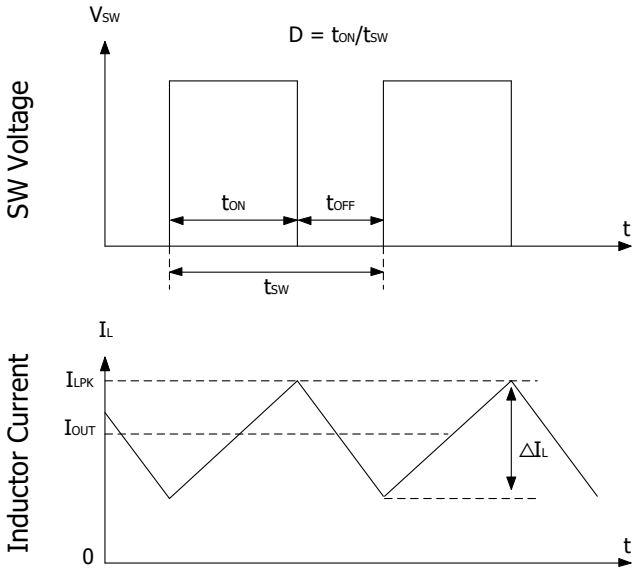


Figure 23. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

DETAILED DESCRIPTION

In continuous conduction mode,ATDC2934 operates at fixed-frequency using peak-current mode control scheme. The controller has an outer voltage feedback loop to get accurate DC voltage regulation. The output of the outer loop is fed to an inner peak-current control loop as reference command that adjusts the peak-current of the inductor. The inductor peak-current is sensed from the high-side switch and is compared to the peak-current reference to control the duty cycle. In other words, as soon as the inductor current reaches the reference peak-current determined by voltage loop, the high-side switch is turned off and the low-side switch is turned on after dead time.

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The voltage feedback loop is internally compensated, which allows for fewer external components, simpler design, and stable operation with almost any combination of output capacitors.

Power-Save Mode

When the load is reduced, the inductor minimum (valley)current eventually reaches zero level (boundary condition).Synchronous rectifier (low-side switch) current is always sensed and when it reaches zero, the controller turns off the low-side switch and does not let the low-side switch sink current. This prevents inductor current from going below zero (negative). This results in discontinuous conduction mode (DCM) operation in which inductor current remains zero until next switching cycle. Both switches are off during this period and do not act as complementary switches. This off-time will extend (that means lower frequency) until output voltage falls below reference voltage again and triggers a new switching cycle. With a new cycle, the high-side switch is turned on again for almost the same t_{ON} time as CCM. Therefore, the output capacitors take almost the same charge in each cycle and with lighter loads it will take longer off-times until output capacitor voltage falls below the reference voltage. The extended off-times mean lower switching frequency that is called frequency foldback and significantly reduces the switching losses, but usually increases the output ripple a little bit.

Note that the on-time of synchronous rectifier switch should always be long enough to fully charge the bootstrap capacitor and prevent bootstrap under voltage lockout due to insufficient voltage for the high-side switch gate driver.

Floating Driver and Bootstrap Charging UVLO Protection

The high-side MOSFET driver is powered by a floating supply provided by an external bootstrap capacitor. The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between BOOT and SW nodes is below regulation, a PMOS pass transistor turns on and connects VIN and BOOT pins internally, otherwise it will turn off. The power supply for the floating driver has its own UVLO protection. The rising UVLO threshold is about 4.7V and with 370mV hysteresis, the falling threshold is about 4.3V. In case of UVLO, the reference voltage of the controller is reset to zero and after recovery a new soft-start process will start.

Output Over-Voltage Protection (OVP)

The ATDC2934 contains an over-voltage comparator that monitors the FB pin voltage. The over-voltage threshold is approximately 110% of nominal FB voltage. When the voltage at the FB pin exceeds the over-voltage threshold (V_{OUT_OV}), PWM switching will be stopped and both high-side and low-side switches will be turned off. If the over-voltage fault is removed,the regulator will automatically recover.

The error amplifier is normally able to maintain regulation since the synchronous output stage has excellent sink and source capability. However it is not able to regulate output when the FB pin is disconnected or when the output is shorted to a higher supply like input supply. Also when V_{OUT} is set to its minimum (0.8V) usually there is no voltage divider and V_{OUT} is directly connected to FB through a resistor (R_1 in the divider) and there is no resistor to ground (no R_2). In such case and with no load, an internal current source of 5μA ~ 6μA from BOOT into the SW pin, which can slowly charge the output capacitor and pull V_{OUT} up to V_{IN}. Therefore a minimum load of at least 10μA must be always present on V_{OUT} (for example an 80kΩ resistor:0.8V/10μA = 80kΩ).

If the FB pin is disconnected, a tiny internal current source will force the voltage at the FB pin to rise above V_{OUT_OV} that triggers over-voltage protection and disables the regulator to protect the loads from a significant over-voltage. Also, if by accident a higher

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external voltage is shorted to the output, V_{FB} will rise above the over-voltage threshold and trigger an OVP event to protect the low-side switch.

DETAILED DESCRIPTION

Minimum High-side On/Off-Time and Frequency Fold-Back

Minimum high-side switch on-time (t_{ON_MIN}) is the smallest duration that the high-side switch can be turned on. The t_{ON_MIN} is typically 100ns. Minimum high-side switch off-time (t_{OFF_MIN}) is the smallest duration that the high-side switch can be turned off. The t_{OFF_MIN} is typically 100ns. In CCM operation, t_{ON_MIN} and t_{OFF_MIN} limit the voltage conversion ratio without switching frequency fold-back. Note that at 1.2MHz the total cycle time is t_{SW} = 833ns.

The minimum and maximum duty cycles without frequency fold-back are given by:

$$D_{MIN} = t_{ON_MIN} \times f_{SW} \quad (1)$$

and

$$D_{MAX} = 1 - t_{OFF_MIN} \times f_{SW} \quad (2)$$

Given a required output voltage, the maximum V_{IN} without frequency fold-back is given by:

$$V_{IN\text{-}MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\text{-}MIN}} \quad (3)$$

and the minimum V_{IN} without frequency fold-back can be calculated by:

$$V_{IN\text{-}MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\text{-}MIN}} \quad (4)$$

Input Voltage

The ATDC2934 can operate efficiently for inputs as high as 42V. For CCM operation (continuous conduction mode) keep duty cycle between 12% and 88%.

Output Voltage

The output voltage can be stepped down to as low as the 0.8V reference voltage (V_{REF}). As explained before, when the output voltage is set to 0.8V and there is no voltage divider, a minimum small load will be needed.An 80kΩ resistor to ground will prevent the output voltage floating up.

Soft-Start

The integrated soft-start circuit in ATDC2934 limits the input inrush current right after power-up or enabling the device. Soft-start is implemented by slowly ramping up the reference voltage that in turn slowly ramps up the output voltage to its target regulation value.

Enable

EN pin turns the ATDC2934 operation on or off. An applied voltage of less than 0.5V shuts down the device, and a voltage of more than 1.2V is required to start the regulator. The EN pin is an input and must not be left open. The simplest way to enable the device is to connect the EN pin to VIN pin via a resistor. This allows for self-startup of the AT2934 when VIN is within the operating range.

An external logic signal can be used to drive the EN input for power savings, power supply sequencing and/or protection. If the EN pin is driven by an external logic signal, a 10kΩ resistor in series with the input is recommended.

Note: Voltage on the EN pin should never exceed V_{IN} +0.3V. Do not drive the EN pin with a logic level if V_{IN} is not present. This can damage the EN pin and the device.

Thermal Shutdown

The ATDC2934 provides an internal thermal shutdown to protect the device when the junction temperature exceeds +150°C. Both switches stop switching in thermal shutdown. Once the die temperature falls

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below +130°C, the device reinitiates the power-up sequence by the internal soft-start.

APPLICATION INFORMATION

External Components

The following guidelines can be used to select external components.

f_{SW} (MHz)	V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	L (μH)	C_{BOOT} (μF)	C_{IN} (μF)	C_{OUT} (μF)
1.2	3.3	31.2	10	10	0.47	10	10
	5	52.5	10	22	0.47	10	22
	12	140	10	47	0.47	10	47

Output Voltage Programming

Output voltage can be set with a resistor divider feedback network between output and FB pin as shown in Figure 4 . Usually, a design is started by selecting lower resistor R_1 and calculating R_2 with the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

where V_{REF} =0.8V.

To keep operating quiescent current small and prevent voltage errors due to leakage currents, it is recommended to choose R1 in the range of 10kΩ to 100kΩ.

If the output has no load other than the FB divider, make sure the divider draws at least 10μA from V_{OUT} or an internal current source (5μA ~ 6μA) from BOOT to SW will slowly charge the output capacitor beyond the desired voltage.

Inductor Selection

The critical parameters for selecting the inductor are the inductance (L), saturation current (I_{sat}) and the maximum RMS current ($I_{rms,max}$) . The inductance is selected based on the desired peak-to-peak ripple current ΔI_L that is given in Equation 6 for CCM. Since the ripple current increases with the input voltage, the maximum input voltage is usually considered to calculate the minimum inductance L_{MIN} that is given in Equation 7. K_{IND} is a design parameter that represents the ratio of inductor ripple current to its maximum operating DC current. Lower K_{IND} means higher inductance value that needs a larger size and higher KIND results in more ripple and loss in the core. Typically, a reasonable value for K_{IND} is around 20%~40%. Inductor peak-current should never exceed the saturation even in transients to avoid over-current protection. Also inductor RMS rating should always be larger than operating RMS current even at maximum ambient temperature.

$$\triangle I_L = \frac{V_{OUT} \times (V_{IN\text{-}MAX} - V_{OUT})}{V_{IN\text{-}MAX} \times L \times f_{SW}} \quad (6)$$

$$L_{MIN} = \frac{V_{IN\text{-}MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\text{-}MAX} \times f_{SW}} \quad (7)$$

where $K_{IND} = \Delta I_L / I_{OUT}$ (max DC current).

Note that lower inductance is usually preferred in a switching power supply, because it usually corresponds to faster transient response and bandwidth, smaller DCR, and reduced size for a more compact design. On the other hand, if the inductance is too small, current ripple will increase which can trigger over-current protection. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. For peak-current mode control, it is recommended to choose large current ripple, because controller comparator performs better with higher signal to noise ratio. So, for this design example, K_{IND} = 0.4 is chosen, and the minimum inductor value is calculated to be 15.3μH. The nearest standard value would be a 22μH ferrite inductor with a 1A RMS current rating and 1.5A saturation current that are well above the designed converter output current RMS and DC respectively.

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Bootstrap Capacitor Selection

The ATDC2934 requires a small external bootstrap capacitor, CBOOT , between the BOOT and SW pins to provide the gate drive supply voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. An X7R or X5R 0.47μF ceramic capacitor with a voltage rating of 16V or higher is recommended for stable operating performance over temperature and voltage variations.

APPLICATION INFORMATION

Input Capacitor Selection

The ATDC2934 requires high frequency input decoupling capacitor(s). The recommended high frequency decoupling capacitor value is 10μF X5R or X7R or higher. It is recommended to choose the voltage rating of the capacitor(s) at least twice the maximum input voltage to avoid derating of the ceramic capacitors with DC voltage. Some bulk capacitances may be needed, especially if the ATDC2934 is not located within 5cm distance from the input voltage source for input stability.

Bulk capacitors have high Equivalent Series Resistance(ESR) and can provide the damping needed to prevent input voltage spiking due to the wiring inductance of the input. The value for this capacitor is not critical but must be rated to handle the maximum input voltage including ripple.

For this design, one 10μF, X7R, 50V is used for the input decoupling capacitor. The ESR is approximately 10mΩ, and the current rating is 1A. To improve high frequency filtering a small parallel 0.1μF capacitor may be placed as close as possible to the device pins.

Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. It is generally desired to use as little outpour capacitance as possible to keep cost and size down and bandwidth high. The output capacitor(s), C_{OUT} , should be chosen carefully since it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during load current transients. The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the ESR of the output capacitors:

$$\Delta V_{OUT_ESR} = \Delta I_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (8)$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$\triangle V_{OUT\text{-}C} = \frac{\triangle I_L}{8 \times f_{SW} \times C_{OUT}} \times \frac{I_{OUT} \times K_{IND}}{8 \times f_{SW} \times C_{OUT}} \quad (9)$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation in presence of large current steps and/or fast slew rate. When a large load step happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The regulator's control loop usually needs 8 or more clock cycles to regulate the inductor current equal to the new load level. The output capacitance must be large enough to supply the current difference for 8 clock cycles to maintain the output voltage within the specified range. Equation 10 shows the minimum output capacitance needed for specified output over/undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times (I_{OH} - I_{OL})}{f_{SW} \times \triangle C_{OUT_SHOOT}} \quad (10)$$

where:

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I_{OL} = Low level of the output current step during load transient.

I_{OH} = High level of the output current during load transient.

V_{OUT_SHOOT} = Target output voltage over/undershoot.

For this design example, the target output ripple is 30mV. Assuming $\Delta V_{OUT_ESR}=\Delta V_{OUT_C}=30mV$, and choosing K_{IND} = 0.4, Equation 8 requires ESR to be less than 125mΩ and Equation 9 requires $C_{OUT}>0.83\mu F$. The target over/undershoot range of this design is ΔV_{OUT_SHOOT} = 5% × V_{OUT} = 250mV. From Equation 10, $C_{OUT}>8\mu F$. So, in summary, the most stringent criteria for the output capacitor is transient constrain of $C_{OUT}>$ 8µF. For the derating margin, one 22µF, 10V, X7R ceramic capacitor with 10mΩ ESR is used.

PCB LAYOUT

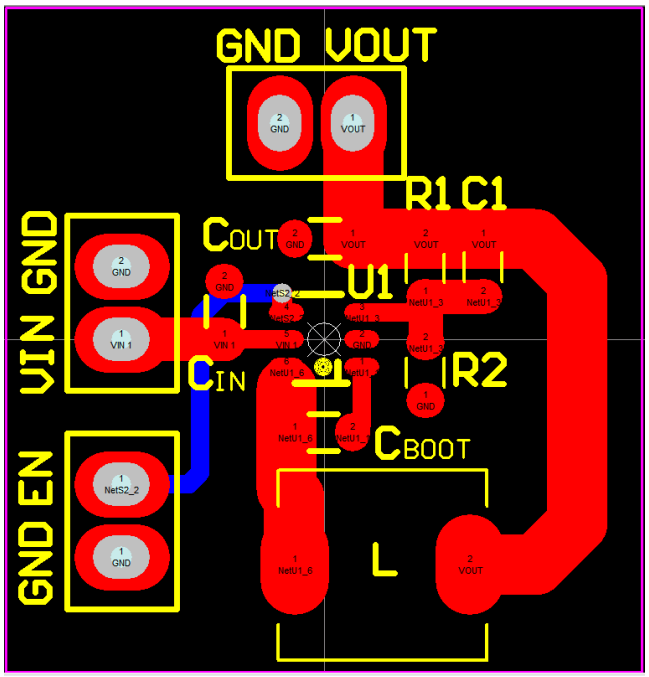


Figure 24. PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 24 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the ATDC2934 VIN and SW pins. The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The SW and BOOST nodes should be as small as possible. Finally, keep the FB nodes small so that the ground traces will shield them from the SW and BOOST nodes. The Exposed Pad on the bottom of the package must be soldered to ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the ATDC2934 to additional ground planes within the circuit board and on the bottom side.

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PACKAGE OUTLINE DUTLINE DIMENSIONS

SOT-23-6

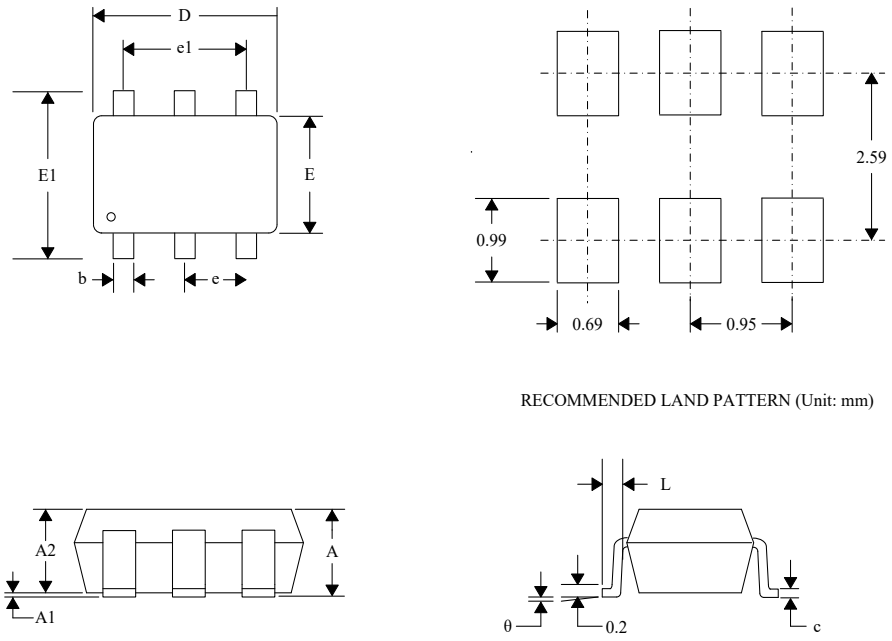
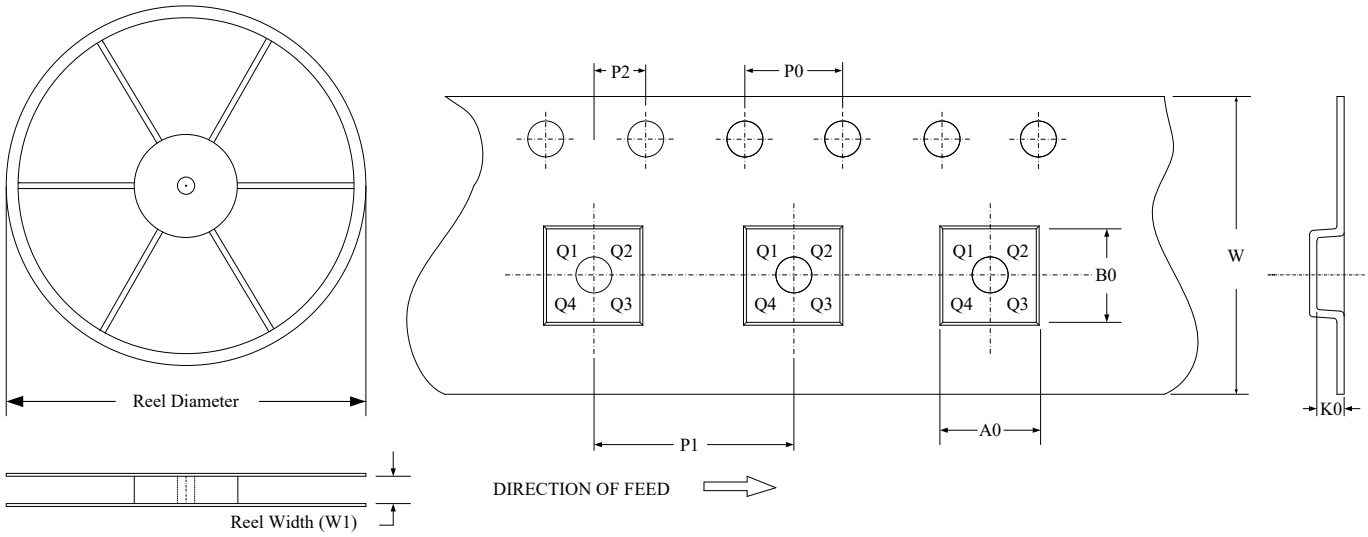


Figure 25. Dimensions

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.05	1.25	0.041	0.049
A1	0.00	0.10	0.000	0.004
A2	1.05	1.15	0.041	0.045
b	0.30	0.50	0.012	0.20
c	0.10	0.20	0.004	0.008
D	2.82	3.02	0.111	0.119
E	1.50	1.70	0.059	0.067
E1	2.65	2.95	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

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TAPE AND REEL INFORMATION

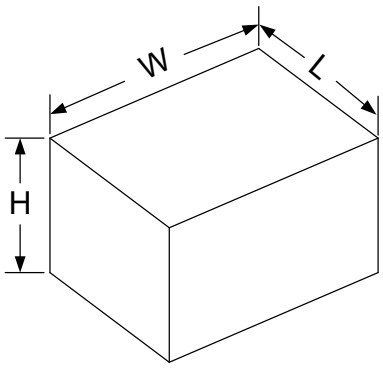


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.17	3.23	1.37	4.0	4.0	2.0	0.8	Q3

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

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Part Number	Buy Now
ATDC2934	* *

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