Zero-Drift RRIO CMOS Operational Amplifier

AT8551

ORDERING GUIDE

Online Stores		Commission Fee	Unit Price (June 2024)	Buy Now
AS	shop.analogtechnologies **Our own online store**	Zero sale commission	$0.90/100PCs	*
SZ	SMTZone **Our own online store**	Zero sale commission	$0.90/100PCs	*
K	Digikey	≈32% sale commission	$1.19/100PCs	*



Figure 1. Physical Photos of AT8551

Table 1. AT8551 vs. AD8551

Parameter		AT8551	AD8551
Offset Voltage		<5μV	10μV
Noise (0.01Hz to 10Hz)		<0.75μV$_{P-P}$	1μV$_{P-P}$
Slew Rate		2.7V/μs	0.4μV/μs
Bandwidth		4.5MHz	1.5MHz
Price	100~499pcs	$0.90	$2.69
	>1000pcs	$0.78	$2.06

FEATURES

- Upgraded Drop-in Replacement for AD8551
- Low Offset Voltage: 1μV (typ) 5μV (max)
- Input Offset Drift: 0.005μV/°C (max)
- High Gain Bandwidth Product: 4.5MHz
- Rail-to-Rail Input and Output
- High Gain, CMRR & PSRR: ≥130dB
- High Slew Rate: 2.7V/μs
- Low Noise: 0.75μV$_{P-P}$ (0.01~10Hz)
- Low Power Consumption: 640μA/op amp
- Overload Recovery Time: 1μs
- Low Supply Voltage: +2.7V to +5.5V
- No External Capacitors Required
- Extended Temperature: −40°C to +125°C

APPLICATIONS

- Temperature & Pressure Sensors Amplifier
- Weight Scale & Strain Gage Amplifiers
- Medical/Industrial Instrumentation
- Handheld Test Equipment
- Precision Current Sensing
- Thermocouple Amplifiers

DESCRIPTION

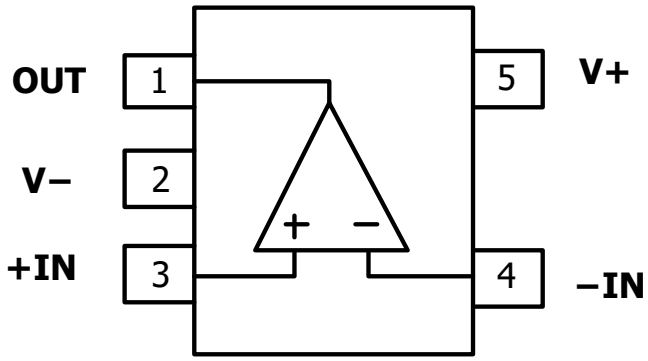
The AT8551 is a general-purpose CMOS operational amplifier that provides ultralow noise, low offset, and low power consumption. The AT8551 uses auto-zero techniques to simultaneously provide very low offset voltage, 5 μV max, and near-zero drift over time and temperature.

This miniature, high-precision operational amplifier offers high input impedance, rail-to-rail input, and rail-to-rail output swing. It features a high gain-bandwidth product of 4.5 MHz and a slew rate of 2.7 V/μs.

This op amp operates from a supply voltage as low as +2.7 V and up to +5.5 V. The AT8551 single amplifier is available in a 5-lead SOT23 package and is specified for the extended industrial and automotive temperature range of −40°C to 125°C.

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026

PIN CONFIGURATIONS



SOT23-5

PIN DESCRIPTION

Descriptions of the pins is listed in Table 2.

Table 2: Pin Function Table for Single OP AMPS

AT8551 SOT23-5	Symbol	Description
1	OUT	Analog Output
2	V−	Negative Power Supply
3	+IN	Noninverting Input
4	−IN	Inverting Input
5	V+	Positive Power Supply
-	NC	No Internal Connection

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, V+ to V−	7.0V
Input Terminals, Voltage (2)	−0.5 to (V+) + 0.5V
Input Terminals, Current (2)	±10mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +125°C
Junction Temperature	150°C
Package Thermal Resistance @ T_A = +25°C	
SOT23-5	200°C/W
MSOP-8, SOIC-8	150°C
Lead Temperature (Soldering, 10s)	260°C
ESD Susceptibility	
HBM	5000V
MM	400V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THERMAL CHARACTERISTICS

Table 5.

Package Type	8-Lead MSOP	8-Lead SOIC	5-Lead SOT23	Unit
$R_{\theta JA}$ Junction-to-ambient thermal resistance	180.3	140.1	220.8	°C/W
$R_{\theta JC}$ (top) Junction-to-case (top) thermal resistance	48.1	89.8	97.5	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	100.9	80.6	61.7	°C/W
ψ_{JT} Junction-to-top characterization parameter	2.4	28.7	7.6	°C/W
ψ_{JB} Junction-to-board characterization parameter	99.3	80.1	61.1	°C/W

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026

ELECTRICAL CHARACTERISTICS

Limits apply over the specified temperature range: T_A = −40°C to +125°C.

(At T_A = +25°C, V_S =5V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.)

Table 6.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = V_S/2 T_A = −40°C to +125°C		1	5	μV
Input Bias Current	I_B	V_{CM} = V_S/2 T_A = −40°C to +125°C		50		pA
Input Offset Current	I_{OS}	T_A = −40°C to +125°C		10		pA
Input Voltage Range	V_{IN}		2.7		5.5	V
Common-Mode Voltage Range	V_{CM}		(V−) − 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	(V−) − 0.1V < V_{CM} < (V+) + 0.1V T_A = −40°C to +125°C	110	130		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	T_A = −40°C to +125°C		0.005	0.05	μV/°C
Channel Separation, dc				0.1		μV/V
Open-Loop Gain	A_{OL}	RL=10kΩ, V_O=0.3V to 4.7V T_A = −40°C to +125°C		110	130	dB
INPUT CAPACITANCE						
Differential				1		pF
Common-Mode				5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100kΩ to GND T_A = −40°C to +125°C	4.99	4.998		V
		R_L = 10kΩ to GND T_A = −40°C to +125°C	4.95	4.98		V
Output Voltage Low	V_{OL}	R_L = 100kΩ to V+ T_A = −40°C to +125°C		1	10	mV
		R_L = 10kΩ to V+ T_A = −40°C to +125°C		10	30	mV
Output Short-Circuit Limit Current	I_{SC}	T_A = −40°C to +125°C		50		mA

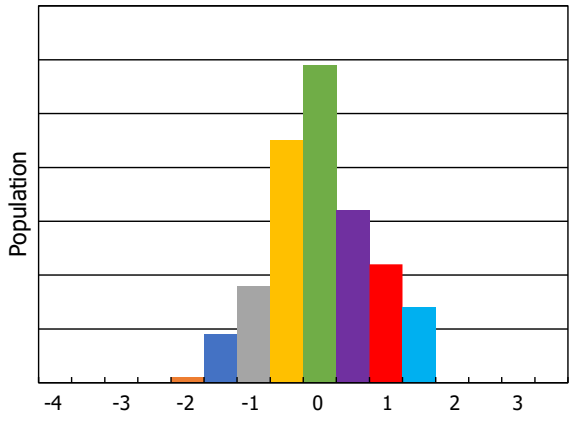
©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.7V to +5.5V, V_{CM} = 0 T_A = −40°C to +125°C	110	130		dB
Quiescent Current/Amplifier	I_Q	V_O = 0 T_A = −40°C to +125°C		640	870	μA
Supply Voltage Range	V_{IN}		2.7		5.5	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	G=+1		2.7		V/μs
Gain Bandwidth Product	GBP			4.5		MHz
Overload Recovery Time				1		μs
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.01Hz to 10Hz		0.75		μV p-p
	e_n p-p	0.01Hz to 1Hz		0.22		μV p-p
Voltage Noise Density	e_n	f = 1kHz		35		nV/√Hz
Current Noise Density	i_n	f = 10Hz		1.5		fA/√Hz

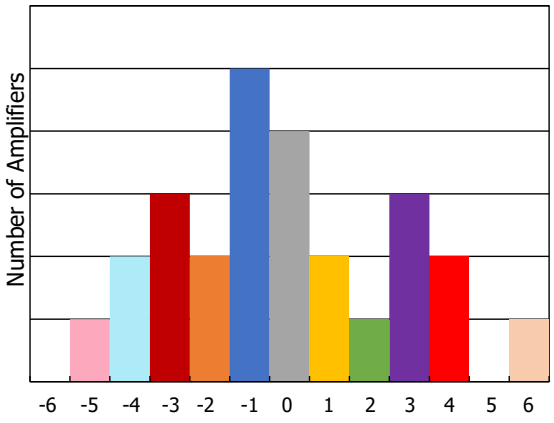
©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026

TYPICAL CHARACTERISTICS

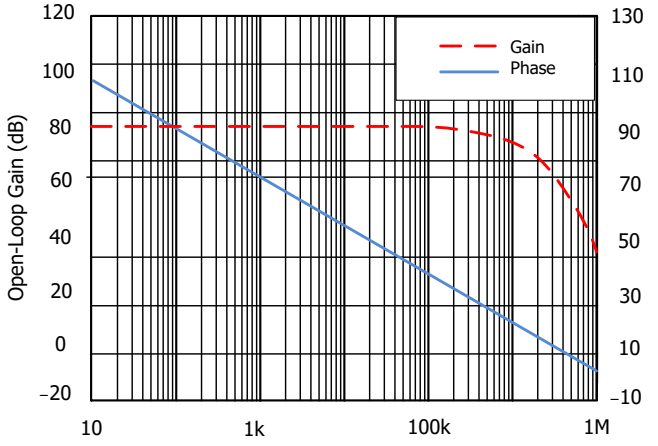
At T_A = +25°C, Vs = 5V, R_{LOAD} = 10kΩ connected to $V_S/2$, V_{OUT} = $V_S/2$, unless otherwise noted.



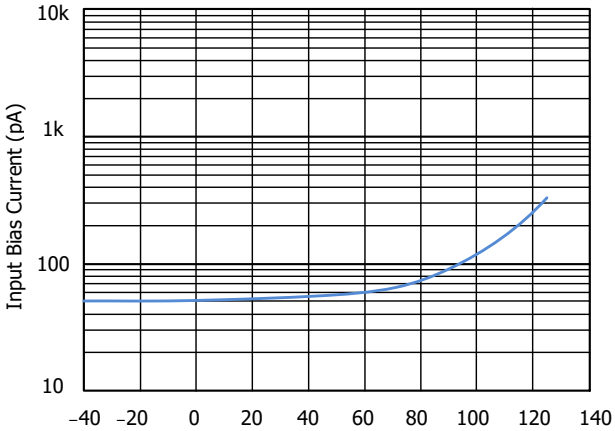
Offset Voltage Production Distribution



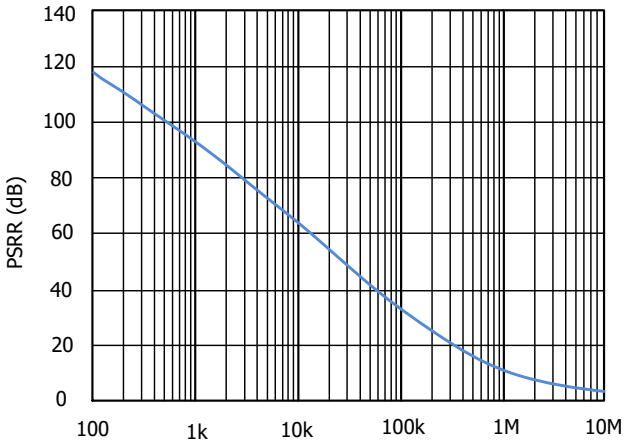
Offset Voltage Drift Production Distribution



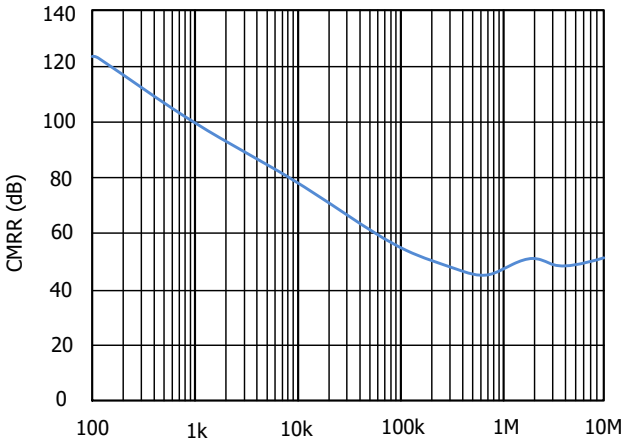
Open-Loop Gain and Phase vs. Frequency



Input Bias Current vs. Temperature

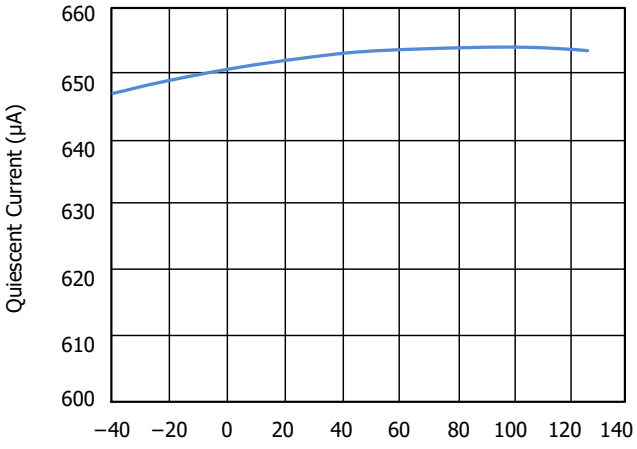


Power-Supply Rejection Ratio vs. Frequency

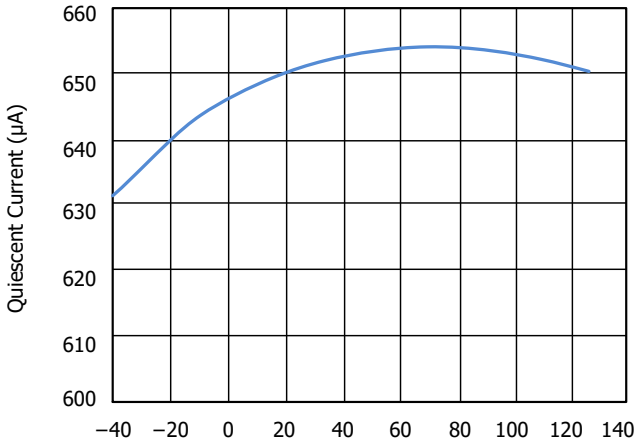


Input Bias Current vs. Temperature

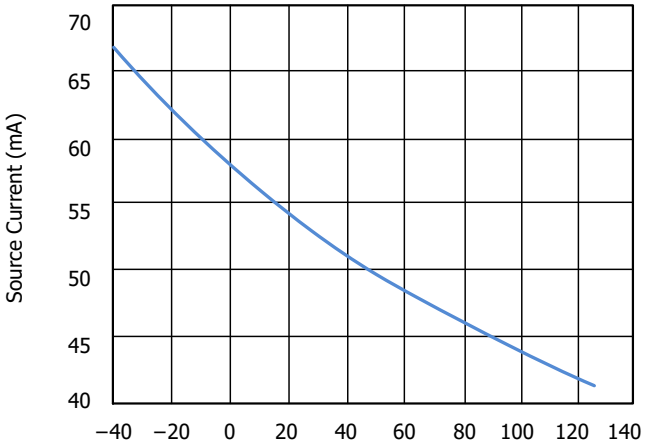
©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026



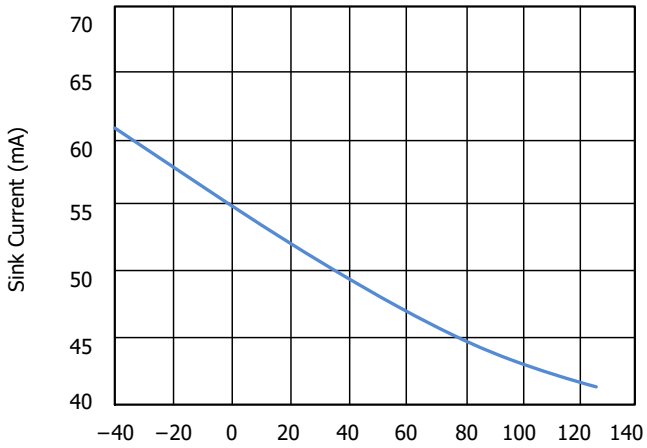
Quiescent Current vs. Temperature



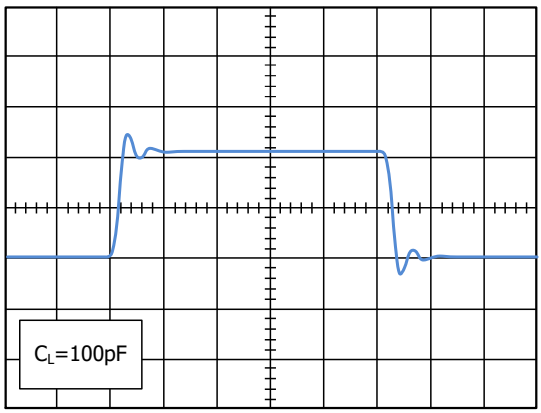
Quiescent Current vs. Temperature



Source Current vs. Temperature

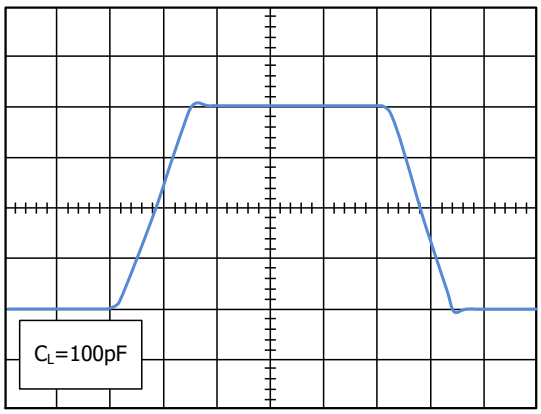


Sink Current vs. Temperature



CH1: 50mV/Div M: 200ns/Div

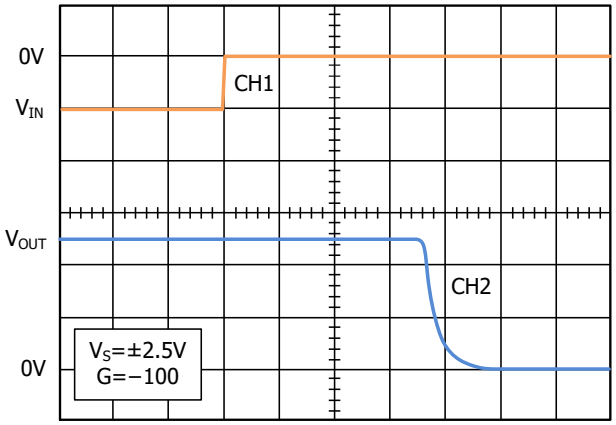
Small−Signal Step Response



CH1: 1V/Div M: 1us/Div

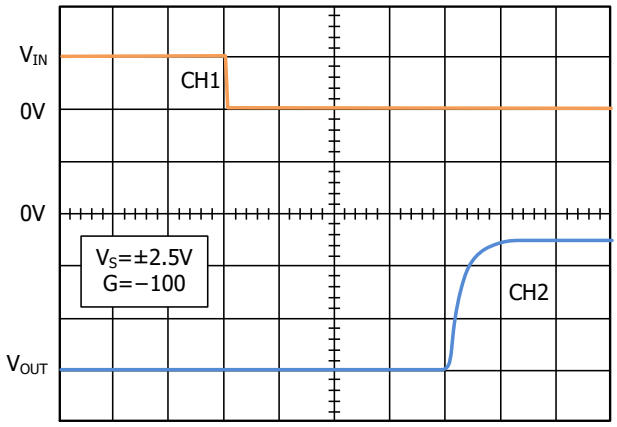
Large−Signal Step Response

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026



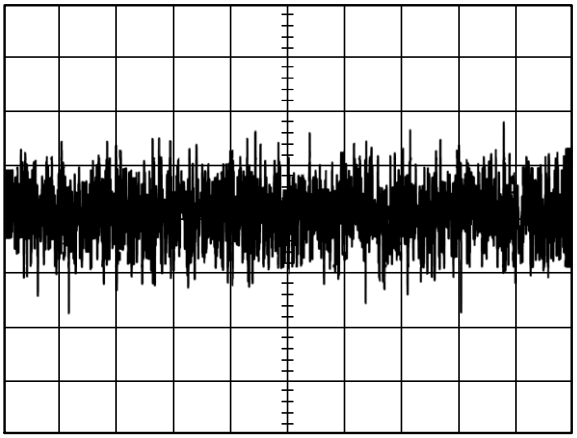
CH1: 200mV/Div CH2: 1V/Div M: 200ns/Div

Positive Overvoltage Recovery



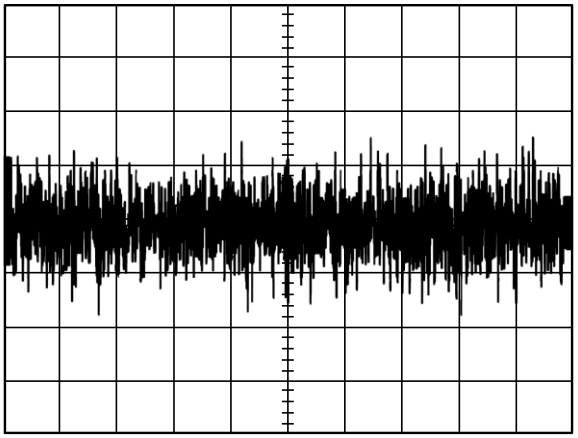
CH1: 200mV/Div CH2: 1V/Div M: 200ns/Div

Positive Overvoltage Recovery



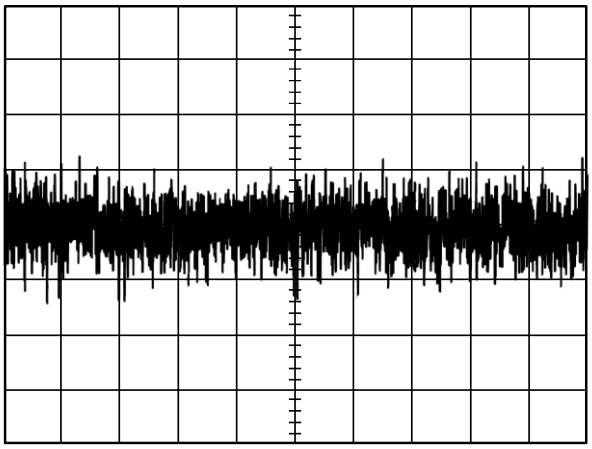
CH1: 200nV/Div M:10s/Div

0.01Hz To 10Hz Noise at Vs = 5V



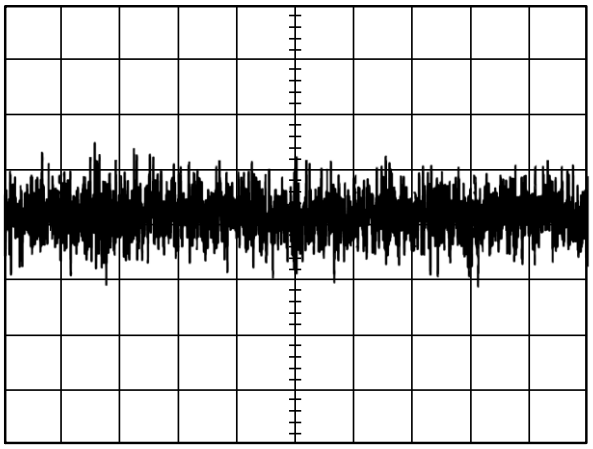
CH1: 400nV/Div M:10s/Div

0.01Hz to 10Hz Noise at Vs = 2.7V



CH1: 100nV/Div M:10s/Div

0.01Hz to 10Hz Noise at Vs = 5V



CH1: 200nV/Div M:10s/Div

0.01Hz to 10Hz Noise at Vs = 2.7V

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026

APPLICATION INFORMATION

The robust design of the AT8551 provides ease-of-use to the circuit designer due to the unity-gain stability, integrated RFI/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection. They use auto zeroing techniques to provide low offset voltage and very low drift over time and temperature. Good layout practice mandates use of a 0.1μF capacitor placed closely across the supply pins. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1μV/°C or higher, depending on materials used.

OPERATING VOLTAGE

The AT8551 operational amplifier family operate over a power supply range of +2.7V to +5.5V. Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. In addition, many specifications apply from –40°C to 125°C. Power supply pins must be bypassed with 0.1μF ceramic capacitors. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this datasheet.

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including: Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry. Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications. Place the external components as close to the device as possible. Place the external components as close to the device as possible. Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit. Consider a driven, low impedance guard ring around the critical traces.

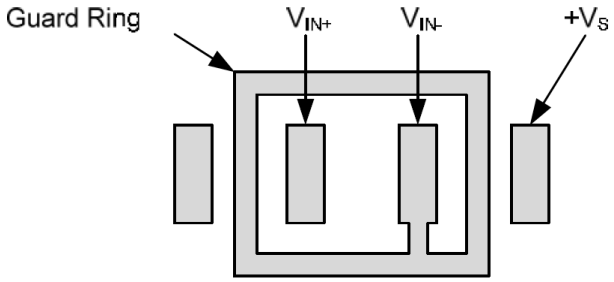
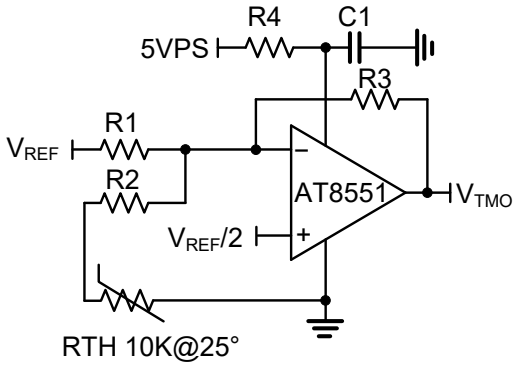


Figure 2. The Layout of Guard Ring

TYPICAL APPLICATION



R1, R2, R3 are TEC temperature control parameters, see Figure 4. Required temperature parameters can be achieved through adjusting R1, R2 and R3, thus TEC controller can detect the temperature range

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026 Email: staff@analogti.com/sales@analogti.com

that users require.

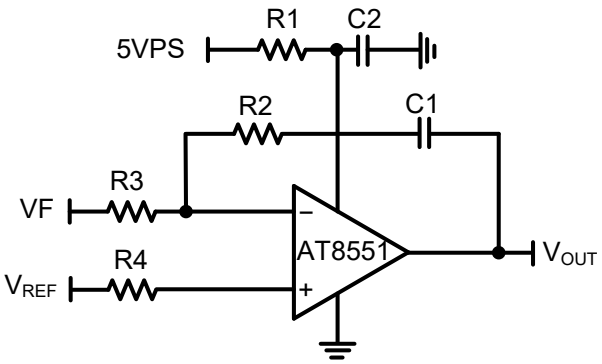
In different temperature ranges, R1, R2 and R3 have different corresponding resistances. R1, R2 and R3 can be determined by:

$$R1 = R_{MID} + \frac{R_{MID}(R_{LOW} + R_{HIGH}) - 2 * R_{LOW} * R_{HIGH}}{R_{LOW} + R_{HIGH} - 2 * R_{MID}}$$

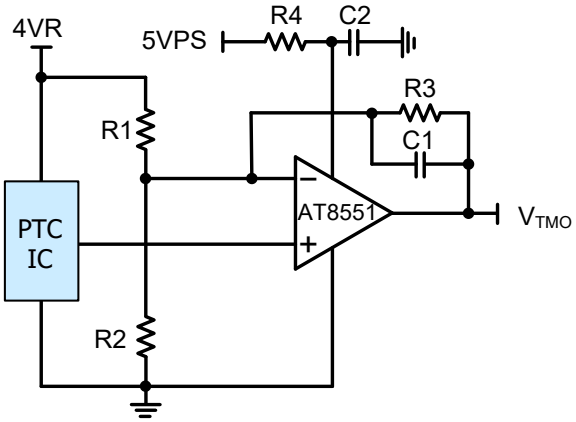
$$R2 = R1 - R_{MID}$$

$$R3 = \frac{R1(R1 + R_{LOW} - R_{MID})}{R_{LOW} - R_{MID}}$$

EA



Positive Coefficient



$V_{TMO}(T_L) = 0.1V$, $V_{TMO}(T_U) = 3.9V$

$$G = \frac{\Delta V_{TMO}}{\Delta V_{PTCIC}} = \frac{V_{TMO}(T_U) - V_{TMO}(T_L)}{V_{PTCIC}(T_U) - V_{PTCIC}(T_L)}$$

$$G = \frac{R3}{R1//R2} + 1$$

$$V_{PTCIC}(T_M) = \frac{V_{PTCIC}(T_U) + V_{PTCIC}(T_L)}{2}$$

$$V_{PTCIC} = V_{PTCIC}(T_M),\ V_{TMO} = \frac{3.9V + 0.1V}{2} = 2V$$

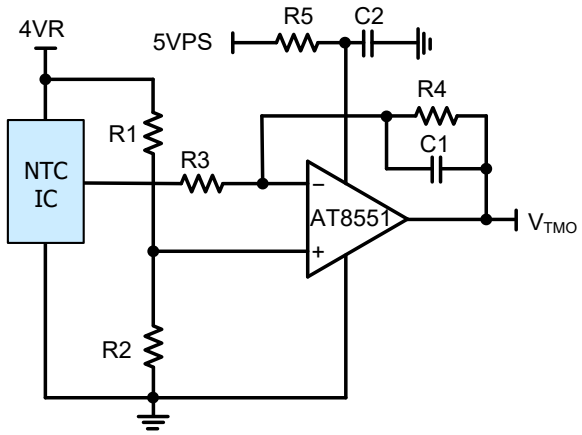
$$\frac{V_{PTCIC}(T_M)}{R2} = \frac{2V - V_{PTCIC}(T_M)}{R3} + \frac{4V - V_{PTCIC}(T_M)}{R1}$$

R3=20kΩ

$$R2 = \frac{R3}{[4V - V_{PTCIC}(T_M)] \times G - 2}$$

$$R1 = \frac{R3}{G - 1 - \frac{R3}{R2}} = \frac{R2 \times R3}{R2 \times (G - 1) - R3}$$

Negative Coefficient



$V_{TMO}(T_L) = 0.1V$, $V_{TMO}(T_U) = 3.9V$

$$G = \frac{\Delta V_{TMO}}{\Delta V_{NTCIC}} = \frac{V_{TMO}(T_U) - V_{TMO}(T_L)}{V_{NTCIC}(T_U) - V_{NTCIC}(T_L)}$$

$$G = \frac{R4}{R3} \qquad R3 = \frac{R4}{G}$$

R4 =20kΩ ~ 200kΩ

$$V_{NTCIC}(T_M) = \frac{V_{NTCIC}(T_U) + V_{NTCIC}(T_L)}{2}$$

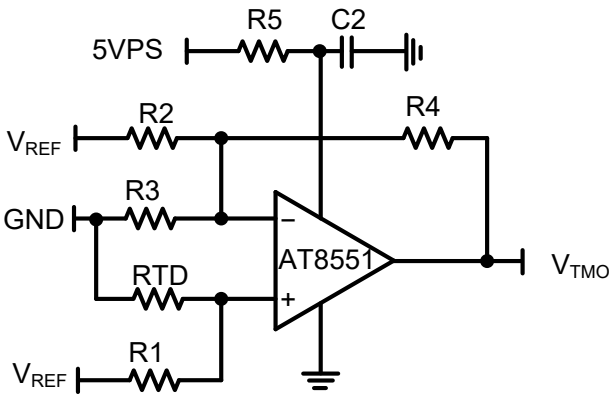
$$\frac{[2V - V_{NTCIC}(T_M)] \times R3}{R3 + R4} + V_{NTCIC}(T_M) = \frac{4V \times R2}{R1 + R2}$$

R2=10k

$$R1 = \frac{40 \times (1 + G)}{2 - V_{NTCIC}(T_M)} - 10$$

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026 Email: staff@analogti.com/sales@analogti.com

RTD



$R_{TD} = R_0 \times (1+0.00385T)$

e.g. $R_0 = 1k\Omega$

When T = 10°C, $R_{TD}(10) = 1.0385k\Omega$

When T = 40°C, $R_{TD}(40) = 1.154k\Omega$

Choose R1

A. $P_{RTD} \leq 1mW$, $R_{TD} = 1000\Omega$

$P_{RTD} = (I_{RTD})^2 \times 1000\Omega = 0.001W$

$$I_{RTD} = 1mA = \frac{4VR}{R1 + R_{TD}} = \frac{4}{R1 + 1k} \Longrightarrow R1=3k\Omega$$

B. $P_{RTD} \leq 1mW$, $R_{TD} = 100\Omega$

$P_{RTD} = (I_{RTD})^2 \times 100\Omega = 0.001W \Longrightarrow$

$$I_{RTD} = 3.16mA = \frac{4VR}{R1 + R_{TD}} = \frac{4}{R1 + 0.1k}$$

R1=1.15kΩ

$$V_{TMO} = \frac{4 \times R_{TD}}{R1 + R_{TD}} \times \left[1 + \frac{R4 \times (R2 + R3)}{R2 \times R3}\right] - \frac{4 \times R4}{R2}$$

I. When T = 10°C, R1 = 3kΩ, $R_{TD}(T_L) = 1.0385k\Omega$,

$$0.93 = \frac{R4 \times (2.97R3 - 1.03R2)}{R2 \times R3}$$

When T = 40°C, R1 = 3kΩ, $R_{TD}(T_U) = 1.154k\Omega$,

$$2.79 = \frac{R4 \times (1.11R2 - 2.89R3)}{R2 \times R3}$$

II. When T = 10°C, R1 = 1.15kΩ, $R_{TD}(T_L) = 1.0385k\Omega$,

$$1.8 = \frac{R4 \times (2.1R3 - 1.9R2)}{R2 \times R3}$$

When T = 40°C, R1 = 1.15kΩ, $R_{TD}(T_U) = 1.154k\Omega$,

$$1.9 = \frac{2 \times R4 \times (R2 - R3)}{R2 \times R3}$$

To achieve the required V_{TMO} outputs at the three different setting point temperatures in the Temperature Network, use the equation:

When T = LOW, RTD = RTD_L, TMO = 0.1V, $V_1 = V_{1L}$

When T = HIGH, RTD = RTD_H, TMO = 4.0V, $V_1 = V_{1H}$

ΔTMO = 4V − 0.1V = 3.9V

$\Delta V1 = V_{1H} - V_{1L}$

$$G = \frac{\Delta TMO}{\Delta V1} = 1 + \frac{R4 \times (R2 + R3)}{R2 \times R3}$$

$RTD = R_0 \times (1+0.00385T)$

e.g. $R_0 = 1k\Omega$

$$V1 = 4.096V \times \frac{RTD}{R1 + RTD}$$

$V_{1L} = 0.5V$

$$R1 = RTD_L \times \frac{4.096V}{V_{1L}} - RTD_L$$

R2 = R1, R3 = RTD_L

$$R4 = (G - 1) \times \frac{R2 \times R3}{R2 + R3}$$

For example, setting the high set-point temperature at 60°C and the low set-point temperature at 0°C.Use $RTD = R_0 \times (1+0.00385T)$, (e.g. $R_0 = 1k\Omega$).

$RTD_L = R_{TD}(10°C) = 1.0k\Omega$

$RTD_H = R_{TD}(60°C) = 1.231k\Omega$

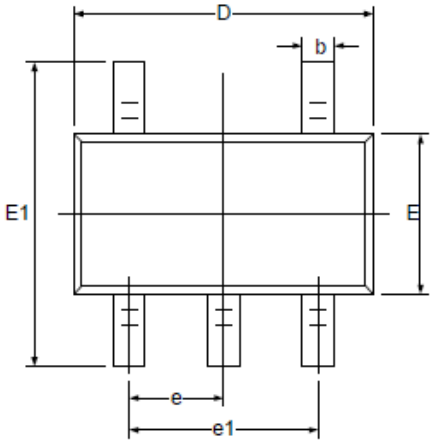
$R_1 = 7.192k\Omega$ $R_2 = R_1 = 7.192k\Omega$

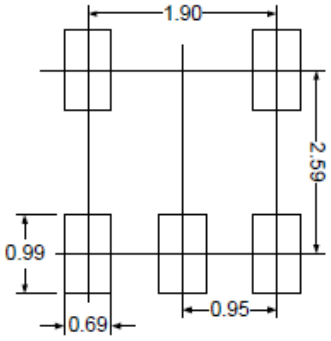
$R_3 = RTD_L = 1.0k\Omega$, $R_4 = 32.308k\Omega$

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026 Email: staff@analogti.com/sales@analogti.com

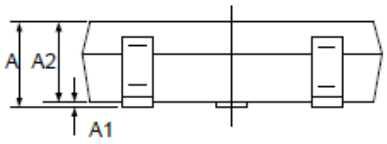
OUTLINE DIMENSIONS

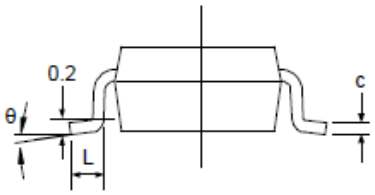
SOT23-5





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026

ORDERING INFORMATION

Part Number	Buy Now
AT8551	* *

*: both and are our online store icons. Our products can be ordered from either one of them with the same pricing and delivery time.

NOTICE

1. ATI warrants performance of its products for one year to the specifications applicable at the time of sale, except for those being damaged by excessive abuse. Products found not meeting the specifications within one year from the date of sale can be exchanged free of charge.
2. ATI reserves the right to make changes to its products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current and complete.
3. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability. Testing and other quality control techniques are utilized to the extent ATI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.
4. Customers are responsible for their applications using ATI products. In order to minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customers to minimize inherent or procedural hazards. ATI assumes no liability for applications assistance or customer product design.
5. ATI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of ATI covering or relating to any combination, machine, or process in which such products or services might be or are used. ATI's publication of information regarding any third party's products or services does not constitute ATI's approval, warranty or endorsement thereof.
6. IP (Intellectual Property) Ownership: ATI retains the ownership of full rights for special technologies and/or techniques embedded in its products, the designs for mechanics, optics, plus all modifications, improvements, and inventions made by ATI for its products and/or projects.

©Copyrights 2000-2026, Analog Technologies, Inc. All Rights Reserved. Updated on 8/11/2026