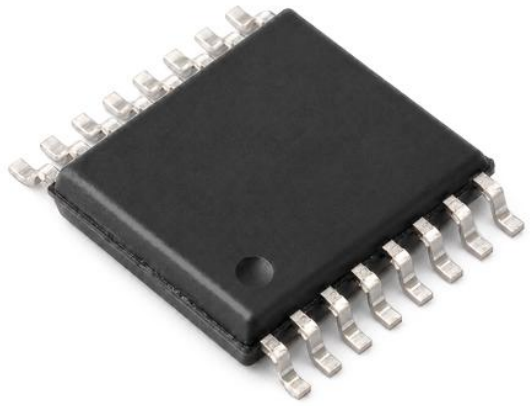


Figure 1. The Physic Photo of AT8254

FEATURES

- High-Precision Voltage Detection for Each Cell
  - Overcharge Detection Voltage n (n = 1 to 4): 3.90V to 4.35V ± 25mV
  - Overcharge Release Voltage n (n = 1 to 4): 3.80V to 4.15V ± 80mV
  - Overdischarge Detection Voltage n (n = 1 to 4): 2.3V to 2.7V ± 80mV
  - Overdischarge Release Voltage n (n = 1 to 4): 2.7V to 3.0V ± 100mV
- 3-level Overcurrent Protection
  - Overcurrent Detection Voltage 1: 0.20V ± 25mV
  - Overcurrent Detection Voltage 2: 0.50V ± 100mV
  - Overcurrent Detection Voltage 3: VC1 – 1.1V ±300mV
- The delay times for disovercharge detection, overcharge detection, and overcurrent detection 1 can be set by external capacitors, while the delay times for overcurrent detection 2 and 3 are internally fixed.
- Charging and discharging operation can be controlled through the control terminals.
- Using high-voltage resistant components with an absolute maximum rating of 26V.
- Wide Operating Voltage Range: 3V to 24V
- Wide Operating Temperature Range: −40°C~85°C
- Low Current Consumption
  - 30μA max. @ working state & T_A= 25°C
  - 0.1μA max. @ standby state & T_A= 25°C
- TSSOP-16 Package

APPLICATIONS

- Lithium-Ion Rechargeable Battery Pack
- Lithium Polymer Rechargeable Battery Pack

DESCRIPTION

The AT8254 series is a protection integrated circuit designed for 3-series or 4-series lithium-ion/lithium polymer rechargeable batteries, including a high precision voltage detector and delay circuit. The AT8254 series can switch between protecting 3-series or 4-series batteries by using the SEL pin.

ABSOLUTE MAXIMUM RATINGS

- VDD – VSS: VSS – 0.3V ~ VSS + 26V
- VMP: VSS – 0.3V ~ VSS + 26V
- DOP: VSS – 0.3V ~ VDD + 0.3V
- COP: VSS – 0.3V ~ VSS + 26V
- Other: VSS – 0.3V ~ VDD + 0.3V
- Power Dissipation: 400mW
- Operating Temperature Range: −40°C ~ 85°C
- Storage Temperature Range: −40°C ~ 125°C

PIN CONFIGURATIONS

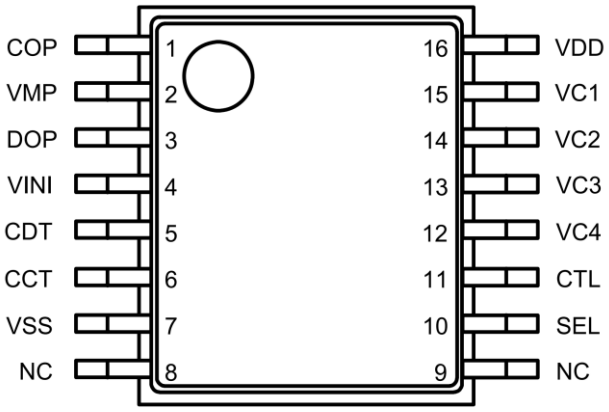


Figure 2. Pin Configuration

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PIN DESCRIPTION

Table 1: Pin Function

Pin #	Symbol	Description
1	COP	MOSFET gate connection pin for charge control (N-channel open-drain output).
2	VMP	Voltage detection pin between VC1 and VMP (Pin for overcurrent detection 3).
3	DOP	MOSFET gate connection pin for discharge control (CMOS output).
4	VINI	Voltage detection pin between VSS and VINI (Pin for overcurrent detection 1, 2).
5	CDT	Capacitor connection for overdischarge detection delay and overcurrent detection 1 delay.
6	CCT	Capacitor connection pin for overcharge detection delay.
7	VSS	Input pin for negative power supply, connection pin for battery 4's negative voltage.
8	NC	No connection.
9	NC	No connection.
10	SEL	Pin for switching 3-series or 4-series cell. VSS level: 3-series cell, VDD level: 4-series cell.
11	CTL	Control pin for the charging MOSFET and the discharging MOSFET.
12	VC4	Connection pin for battery 3's negative input & battery 4's positive input.
13	VC3	Connection pin for battery 2's negative input & battery 3's positive input.
14	VC2	Connection pin for battery 1's negative input & battery 2's positive input.
15	VC1	Connection pin for battery 1's positive input.
16	VDD	Input pin for positive power supply, connection pin for battery 1's positive voltage.

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BLOCK DIAGRAM

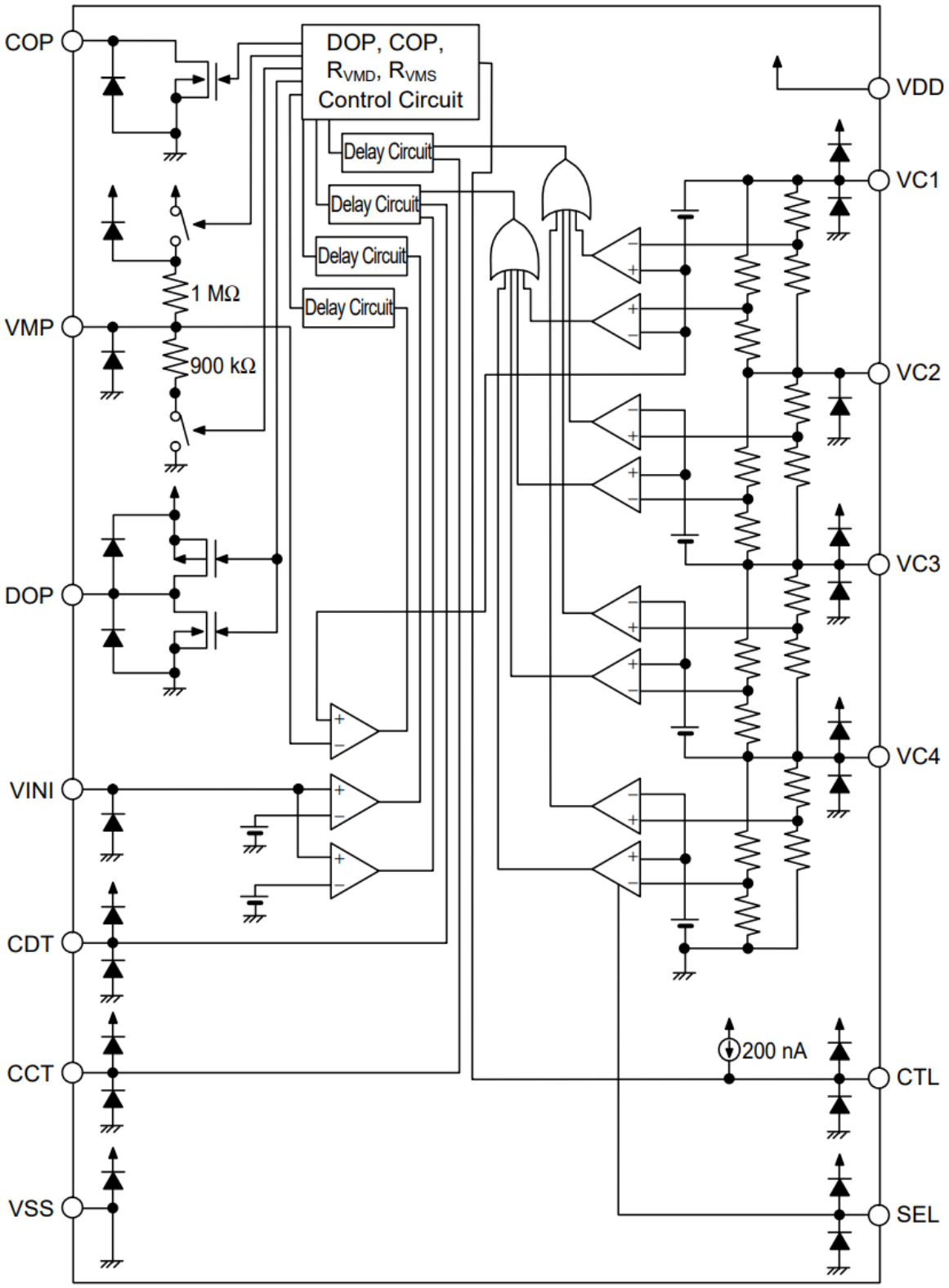


Figure 2. Block Diagram

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ELECTRICAL CHARACTERISTICS

(At T_A = +25°C, V_{IN} = 12V, unless otherwise noted.)

Table 3.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n (n = 1, 2, 3, 4)	V_{CUn}		V_{CUn}−0.025	V_{CUn}	V_{CUn}+0.025	V	2
Overcharge release voltage n (n = 1, 2, 3, 4)	V_{CLn}		V_{CLn}−0.08	V_{CLn}	V_{CLn}+0.08	V	2
Overdischarge detection voltage n (n = 1, 2, 3, 4)	V_{DLn}		V_{DLn}−0.08	V_{DLn}	V_{DLn}+0.08	V	2
Overdischarge release voltage n (n = 1, 2, 3, 4)	V_{DUn}		V_{DUn}−0.10	V_{DUn}	V_{DUn}+0.10	V	2
Overcurrent detection voltage 1	V_{IOV1}		V_{IOV1}−0.025	V_{IOV1}	V_{IOV1}+0.025	V	2
Overcurrent detection voltage 2	V_{IOV2}		0.4	0.5	0.6	V	2
Overcurrent detection voltage 3	V_{IOV3}		V_{C1}−1.5	V_{C1}−1.2	V_{C1}−0.9	V	2
Delay Time							
Overcharge detection delay time	t_{CU}	CCT pin capacitance = 0.1μF	0.5	1.0	1.5	s	3
Overdischarge detection delay time	t_{DL}	CDT pin capacitance = 0.1μF	50	100	150	ms	3
Overcurrent detection delay time 1	t_{IOV1}	CDT pin capacitance = 0.1μF	5	10	15	ms	3
Overcurrent detection delay time 2	t_{IOV2}		0.4	1	1.6	ms	3
Overcurrent detection delay time 3	t_{IOV3}	FET gate capacitance = 2000pF	100	300	600	μs	3
0V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled		0.8	1.5	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge inhibited	0.4	0.7	1.1	V	4
Internal Resistance							
Resistance between VMP and VDD	R_{VMD}		0.5	1	1.5	MΩ	5
Resistance between VMP and VSS	R_{VMS}		450	900	1800	kΩ	5

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Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Input Voltage							
Operating voltage between VDD and VSS	V_{DSOP}	Output voltage of DOP and COP fixed	3		24	V	2
CTL input voltage "H"	V_{CTLH}		V_{DD}×0.8			V	2
CTL input voltage "L"	V_{CTLL}				V_{DD}×0.2	V	2
SEL input voltage "H"	V_{SELH}		V_{DD}×0.8			V	2
SEL input voltage "L"	V_{SELL}				$_{VDD}$×0.2	V	2
Input Current							
Current consumption during operation	I_{OPE}	V1=V2=V3=V4=3.5V		12	30	μA	1
Current consumption during power-down	I_{PDN}	V1=V2=V3=V4=1.5V			0.1	μA	1
VC1 pin current	I_{VC1}	V1=V2=V3=V4=3.5V		1.5	3	μA	5
VC2 pin current	I_{VC2}	V1=V2=V3=V4=3.5V	−0.3	0	0.3	μA	5
VC3 pin current	I_{VC3}	V1=V2=V3=V4=3.5V	−0.3	0	0.3	μA	5
VC4 pin current	I_{VC4}	V1=V2=V3=V4=3.5V	−0.3	0	0.3	μA	5
CTL pin current "H"	I_{CTLH}	V1=V2=V3=V4=3.5V V_{CTL} = V_{DD}			0.1	μA	5
CTL pin current "L"	I_{CTLL}	V1=V2=V3=V4=3.5V V_{CTL} = V_{SS}	−0.4	−0.2		μA	5
SEL pin current "H"	I_{SELH}	V1=V2=V3=V4=3.5V V_{SEL} = V_{DD}			0.1	μA	5
SEL pin current "L"	I_{SELL}	V1=V2=V3=V4=3.5V V_{SEL} = V_{SS}	0.1			μA	5
Output Current							
COP pin leakage current	I_{COH}	V_{COP} = 24V			0.1	μA	5
COP pin sink current	I_{COL}	V_{COP} = V_{SS} + 0.5V	10			μA	5
DOP pin source current	I_{DOH}	V_{DOP} = V_{DD} − 0.5V	10			μA	5
DOP pin sink current	I_{DOL}	V_{DOP} = V_{SS} + 0.5V	10			μA	5

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TEST CIRCUITS

1. Current Consumption during Operation &Current Consumption during Power-down

(Test circuit 1)

The current at the VSS pin is the current consumption during operation (IOPE), when V1 = V2 = V3 = V4 = 3.5V and $V_{VMP} = V_{DD}$.

The current at the VSS pin is the current consumption during power-down (IPDN), when V1 = V2 = V3 = V4 = 1.5V and $V_{VMP} = V_{SS}$.

2. Overcharge Detection Voltage, Overcharge Release Voltage, Overdischarge Detection Voltage, Overdischarge Release Voltage, Overcurrent Detection Voltage 1, Overcurrent Detection Voltage 2, Overcurrent Detection Voltage 3, CTL Input Voltage "H", CTL Input Voltage "L", SEL Input Voltage "H", SEL Input Voltage "L".

(Test circuit 2)

Confirm that the COP pin and DOP pin are low (V_{DD} × 0.1V or lower) when $V_{VMP} = V_{SEL} = V_{DD}$, $V_{INI} = V_{CTL} = V_{SS}$, the CCT pin is open, the CDT pin is open, and V1 = V2 = V3 = V4 = 3.5V (this status is referred to as the initial status).

- Overcharge Detection Voltage (V_{CU1}), Overcharge Release Voltage (V_{CL1})

  The overcharge detection voltage (V_{CU1}) is the voltage of V1 when the voltage of the COP pin is "H" (VDD × 0.9V or more) after the V1 voltage has been gradually increased starting at the initial status. The overcharge release voltage (V_{CL1}) is the voltage of V1 when the voltage at the COP pin is "L" after the V1 voltage has been gradually decreased.

- Overdischarge Detection Voltage (V_{DL1}), Overdischarge Release Voltage (V_{DU1})

  The overdischarge detection voltage (V_{DL1}) is the voltage of V1 when the voltage of the DOP pin is "H" after the V1 voltage has been gradually decreased starting at the initial status. The overdischarge release voltage (V_{DU1}) is the voltage of V1 when the voltage at the DOP pin is "L" after the V1 voltage has been gradually increased. When the voltage of Vn (n = 2 to 4) is changed, the overcharge detection voltage (V_{CUn}), overcharge release voltage (V_{CLn}), overdischarge detection voltage (V_{DLn}), and overdischarge release voltage (V_{DUn}) can be determined in the same way as when n = 1.

- Overcurrent Detection Voltage 1 (V_{IOV1})

  Overcurrent detection voltage 1 (V_{IOV1}) is the voltage of the VINI pin when the voltage of the DOP pin is "H" after the VINI pin voltage has been gradually increased starting at the initial status.

- Overcurrent Detection Voltage 2 (V_{IOV2})

  Overcurrent detection voltage 2 (V_{IOV2}) is the voltage of the VINI pin when the voltage of the DOP pin is "H" after the voltage of the CDT pin was set to V_{SS} following the initial status and the voltage of the VINI pin has been gradually decreased.

- Overcurrent Detection Voltage 3 (V_{IOV3})

  Overcurrent detection voltage 3 (V_{IOV3}) is the voltage difference between V_{VC1} and V_{VMP} ($V_{VC1} - V_{VMP}$) when the voltage of the DOP pin is "H" after the VMP voltage has been gradually decreased starting at the initial status.

- CTL Input Voltage "H" (V_{CTLH}), CTL Input Voltage "L" (V_{CTLL})

  The CTL input voltage "H" (V_{CTLH}) is the voltage of CTL when the voltages at the COP and DOP pins are "H" after the CTL voltage has been gradually increased starting at the initial status. The CTL input voltage "L" (V_{CTLL}) is the voltage of CTL when the voltages at the COP and DOP pins are "L" after the CTL voltage has been gradually decreased.

- SEL Input Voltage "H" (V_{SELH}), SEL Input Voltage "L" (V_{SELL})

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Apply 0 V to V4 in the initial status and confirm that the DOP pin is "H". The SEL input voltage "L" (V_{SELL}) is the voltage of the SEL pin when the voltage at the DOP pin is "L" after the SEL voltage has been gradually decreased. The SEL input voltage "H" (V_{SELH}) is the voltage of the SEL pin when the voltage of the DOP pin is "H" after the SEL voltage has been gradually increased.

3. Overcharge Detection Delay Time, Overdischarge Detection Delay Time, Overcurrent Detection Delay Time 1, Overcurrent Detection Delay Time 2, Overcurrent Detection Delay Time 3.

(Test circuit 3)

Confirm that the COP pin and DOP pin are "L" when $V_{VMP} = V_{DD}$, $V_{INI} = V_{SS}$, and V1 = V2 = V3 = V4 = 3.5V (this status is referred to as the initial status).

- Overcharge Detection Delay Time (t_{CU})

  The overcharge detection delay time (tCU) is the time it takes for the voltage of the COP pin to change from "L" to "H" after the voltage of V1 is instantaneously changed to 4.5V from the initial status.

- Overdischarge Detection Delay Time (t_{DL})

  The overdischarge detection delay time (t_{DL}) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of V1 is instantaneously changed to 1.5V from the initial status.

- Overcurrent Detection Delay Time 1 (t^{IOV1})

  Overcurrent detection delay time 1 (t_{IOV1}) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of the VINI pin is instantaneously changed to 0.4V from the initial status.

- Overcurrent Detection Delay Time 2 (t_{IOV2})

  Overcurrent detection delay time 2 (t_{IOV2}) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of the VINI pin is instantaneously changed to V_{IOV2_max} + 0.2V from the initial status.

- Overcurrent Detection Delay Time 3 (t_{IOV3})

  Overcurrent detection delay time 3 (t_{IOV3}) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of the VMP pin is instantaneously changed to V_{IOV3_min} − 0.2V from the initial status.

4. 0V Battery Charge Starting Charger Voltage (0V Battery Charge Enabled), 0V Battery Charge Inhibition Battery Voltage (0V Battery Charge Inhibited)

(Test circuit 4)

Either the 0V battery charge starting charger voltage or the 0V battery charge inhibition battery voltage is applied to each product according to the 0V battery charge function.

- For the 0 V battery charge starting charger voltage, the COP pin voltage should be lower than $V_{0CHA_max.}$ − 1V when V1 = V2 = V3 = V4 = 0V and $V_{VMP} = V_{0CHA_max}$.
- For 0 V battery charge inhibition battery voltage, the COP pin voltage should be higher than V_{VMP} −1V when V1 = V2 = V3 = V4 = V_{0INH_min} and $V_{VM}P$ = 24 V.

5. Resistance between VMP and VDD, Resistance between VMP and VSS, VC1 Pin Current, VC2 Pin Current, VC3 Pin Current, VC4 Pin Current, CTL pin Current "H", CTL Pin Current "L", SEL Pin Current "H", SEL Pin Current "L", COP Pin Leakage Current, COP Pin Sink Current, DOP Pin Source Current, DOP Pin Sink Current.

(Test circuit 5)

$V_{VMP} = V_{SEL} = V_{DD}$, $V_{INI} = V_{CTL} = V_{SS}$, V1 = V2 = V3 = V4 = 3.5V, and other pins left "open" (this status is referred to as the initial status).

- The resistance between VMP and VDD (R_{VMD}) is obtained from $R_{VMD} = V_{DD} / I_{VMD}$ using the current value of the VMP pin (I_{VMD}) when $V_{VMP} = V_{SS}$ after the initial status.

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- The resistance between VMP and VSS (R_{VMS}) is obtained from $R_{VMS} = V_{DD} / I_{VMS}$ using the current value of the VMP pin (I_{VMS}) when V1 = V2 = V3 = V4 = 1.8V after the initial status.
- At the initial status, the current that flows through the VC1 pin is the VC1 pin current (I_{VC1}), the current that flows through the VC2 pin is the VC2 pin current (I_{VC2}), the current that flows through the VC3 pin is the VC3 pin current (I_{VC3}), and the current that flows through the VC4 pin is the VC4 pin current (I_{VC4}).
- In the initial status, the current that flows through the CTL pin is the CTL pin current "L" (I_{CTLL}), after that, when $V_{CTL} = V_{DD}$, the current that flows through the CTL pin is the CTL pin current "H" (I_{CTLH}).
- In the initial status, the current that flows through the SEL pin is the SEL pin current "H" (I_{SELH}), after that, when $V_{SEL} = V_{SS}$, the current that flows through the SEL pin is the SEL pin current "L" (I_{SELL}).
- The COP pin sink current (I_{COL}) is the current that flows through the COP pin when $V_{COP} = V_{SS} + 0.5V$ after the initial status. After that, the current that flows through the COP pin when V1 = V2 = V3 = V4 = 6V and $V_{COP} = V_{DD}$ is the COP pin leakage current (I_{COH}).
- The DOP pin sink current (I_{DOL}) is the current that flows through the DOP pin when $V_{DOP} = V_{SS} + 0.5V$ after the initial status. After that, the current that flows through the DOP pin when $V_{VMP} = V_{DD} - 2V$ and $V_{DOP} = V_{DD} - 0.5V$ is the DOP pin source current (I_{DOH}).

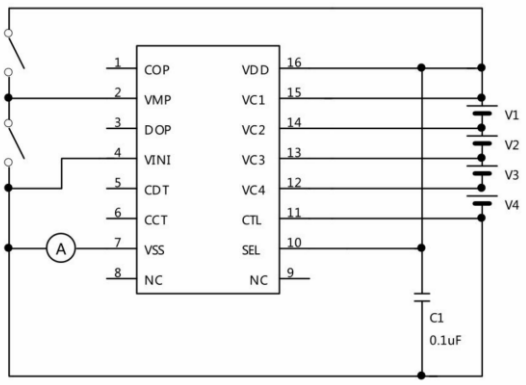


Figure 3. Test Circuit 1

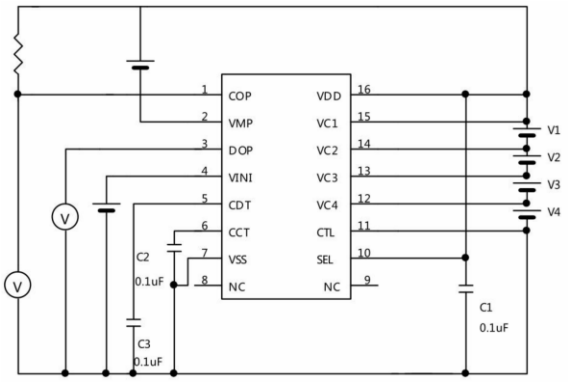


Figure 5. Test Circuit 3

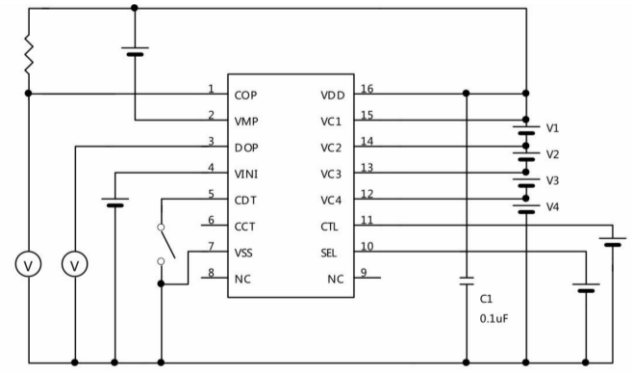


Figure 4. Test Circuit 2

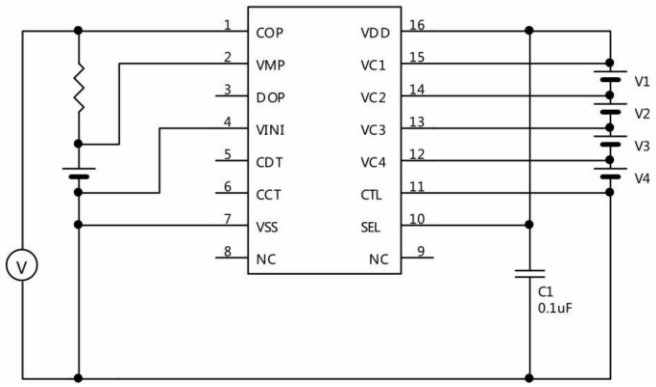


Figure 6. Test Circuit 4

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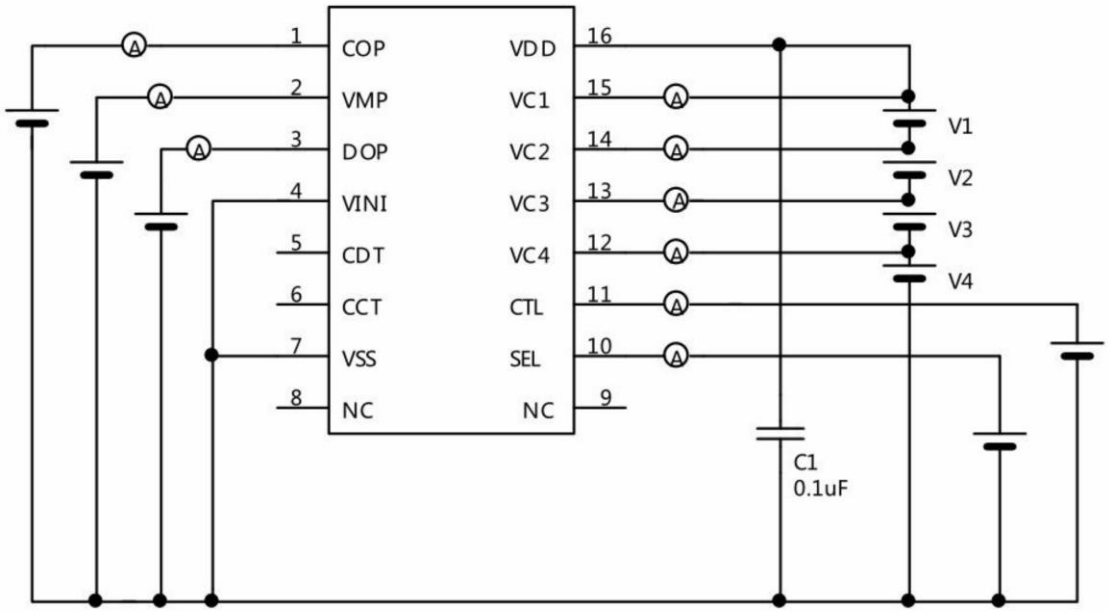


Figure 7. Test Circuit 5

INSTRUCTION

1. Normal Status

When the voltage of each of the batteries is in the range from V_{DLn} to V_{CUn} and the discharge current is lower than the specified value (the VINI pin voltage is lower than V_{IOV1} and V_{IOV2}, and the VMP pin voltage is higher than V_{IOV3}), the charging and discharging FETs are turned on.

2. Overcharge Status

When the voltage of one of the batteries becomes higher than V_{CUn} and the state continues for t_{CU} or longer, the COP pin becomes high impedance. The COP pin is pulled up to the EB+ pin voltage by an external resistor, and the charging FET is turned off to stop charging. This is called the overcharge status. The overcharge status is released when one of the following two conditions holds.

(1). The voltage of each of the batteries becomes V_{CLn} or lower.

(2). The voltage of each of the batteries is V_{CUn} or lower, and the VMP pin voltage is 39/40 × VDD or lower (a load is connected and discharging is started via the body diode of the charging FET).

3. Overdischarge Status

When the voltage of one of the batteries becomes lower than V_{DLn} and the state continues for t_{DL} or longer, the DOP pin voltage becomes VDD level, and the discharging FET is turned off to stop discharging. This is called the overdischarge status.

4. Overcurrent Status

The AT8254 Series has three overcurrent detection levels (V_{IOV1}, V_{IOV2}, and V_{IOV3}) and three overcurrent detection delay times (t_{IOV1}, t_{IOV2}, and t_{IOV3}) corresponding to each overcurrent detection level. When the discharging current becomes higher than the specified value (the voltage between VSS and VINI is greater than V_{IOV1}) and the state continues for t_{IOV1} or longer, the AT8254 Series enters the overcurrent status, in which the DOP pin voltage becomes VDD level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to the EB+ pin voltage to turn off the charging FET to stop charging, and the VMP pin is pulled up to the VDD voltage by the internal resistor (R_{VMD}). Operation of overcurrent detection level 2 (V_{IOV2}) and overcurrent detection delay time 2 (t_{IOV2}) is the same as for V_{IOV1} and t_{IOV1}. In the overcurrent status, the VMP pin is pulled up to the VDD level by the internal resistor in the IC (RVMD resistor). The overcurrent status is released when the following condition holds.

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(1) The VMP pin voltage is V_{IOV3} or higher because a charger is connected or the load (30MΩ or more) is released.

5. Delay Time Setting

The overcharge detection delay time (t_{CU}) is determined by the external capacitor connected to the CCT pin. The overdischarge detection delay time (t_{DL}) and overcurrent detection delay time 1 (t_{IOV1}) are determined by the external capacitor connected to the CDT pin. Overcurrent detection delay times 2 and 3 (t_{IOV2}, t_{IOV3}) are fixed internally.

min. typ. max.

t_{CU}[s] = (5.00, 10.0, 15.0) × C_{CCT}[μF]

t_{DL}[s] = (0.50, 1.00, 1.50) × C_{CDT}[μF]

t_{IOV1}[s] = (0.05, 0.10, 0.15) × C_{CDT}[μF]

6. Dormant State

When transitioning to over-discharge status, discharge ceases. As the internal RVMS resistor within the IC pulls the VMP terminal to VSS, the voltage on the VMP terminal drops below VDD/2, causing the SLM8254 to enter a dormant state. In this state, nearly all circuits within the SLM8254 stop functioning, reducing the current consumption to below IPDN. The status of each output terminal becomes as follows:

(1) COP Hi-Z

(2) DOP VDD

The dormant state is terminated under the following conditions:

(1) The voltage on the VMP terminal rises above V_{DD}/2 (charger connected).

(2) All battery voltages rise above V_{DLn}, and the VDD sub-voltage rises above V_{DD}/2 (charger connected).

7. 0V Battery Charge

Regarding charging of the battery after self-discharge (0V battery), the SLM8254 allows charging of the 0V battery (which can be charged to the 0V battery).Caution When the VDD pin voltage is lower than the minimum value of V_{DSOP}, the operation of the AT8254 Series is not guaranteed.

8. CTL Pin

The AT8254 Series has control pins. The CTL pin is used for controlling the COP and DOP pin output voltages. CTL pin takes precedence over the battery protection circuit.

CTL	COP	DOP
High	Hi-Z	VDD
Open	Hi-Z	VDD
Low	Normal	Normal

9. SEL pin

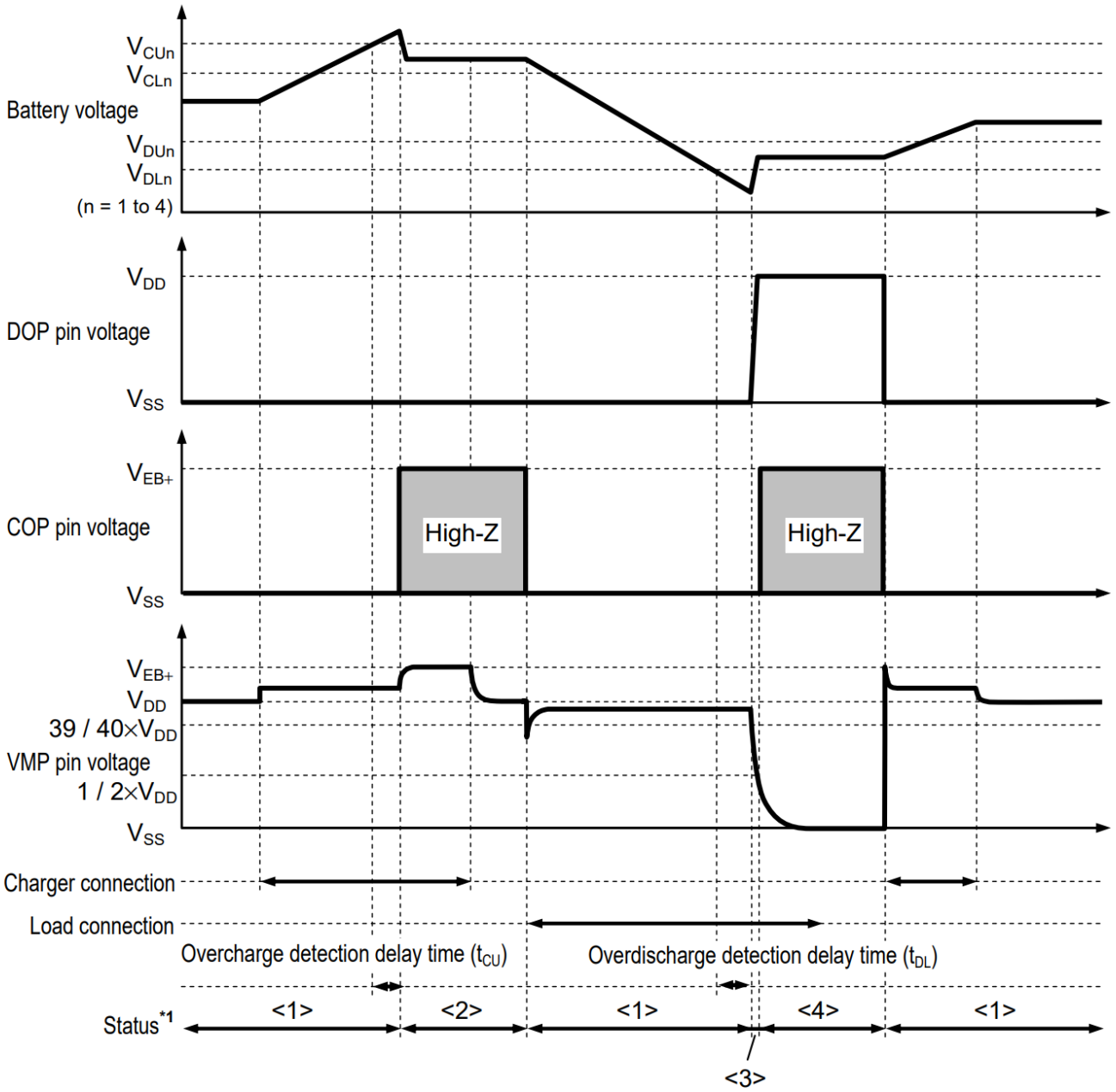
The AT8254 Series has control pins. The SEL pin is used for switching between 3-cell and 4-cell protection. When the SEL pin is low, overdischarge detection of the V4 cell is prohibited and an overdischarge is not detected even if the V4 cell is shorted, therefore, this IC can be used for 3-cell protection. The SEL pin takes precedence over the battery protection circuit. Use the SEL pin at high or low.

SEL	State
High	4-cell protection
Open	Undefined
Low	3-cell protection

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TIMING CHART

1. Overcharge Detection and Overdischarge Detection



Note:

(1). Normal status

(2). Overcharge status

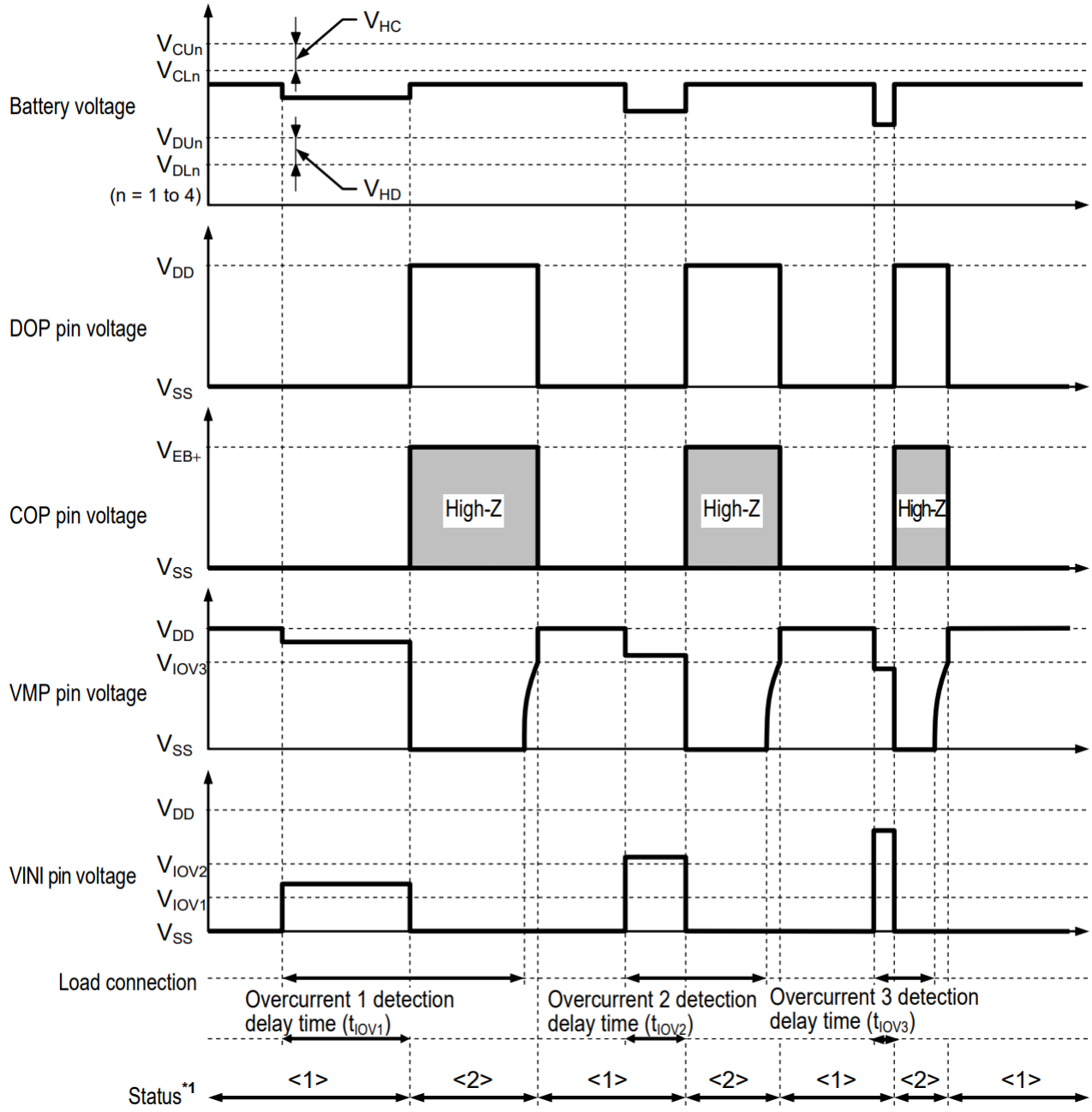
(3). Overdischarge status

(4). Power-down status

The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

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2. Overcurrent Detection



Note:

(1). Normal status

(2). Overcurrent status

The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

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TYPICAL APPLICATION

3-serial Cell

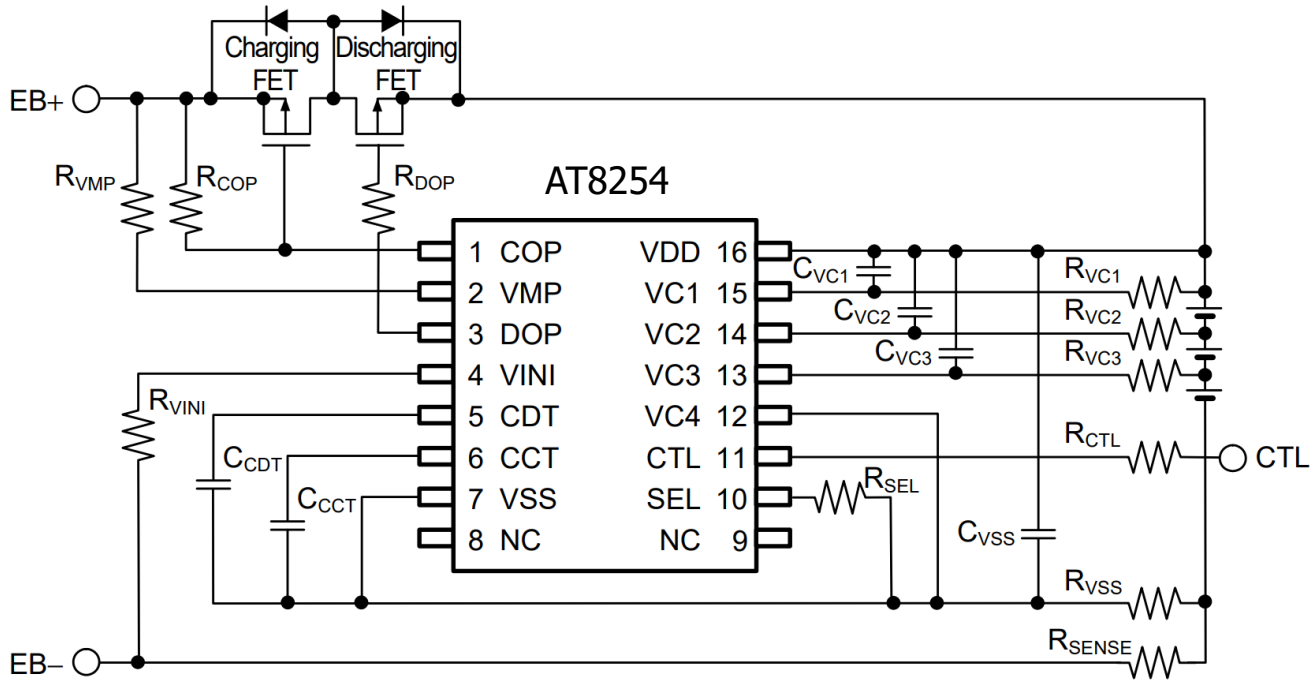


Figure 8.

4-serial Cell

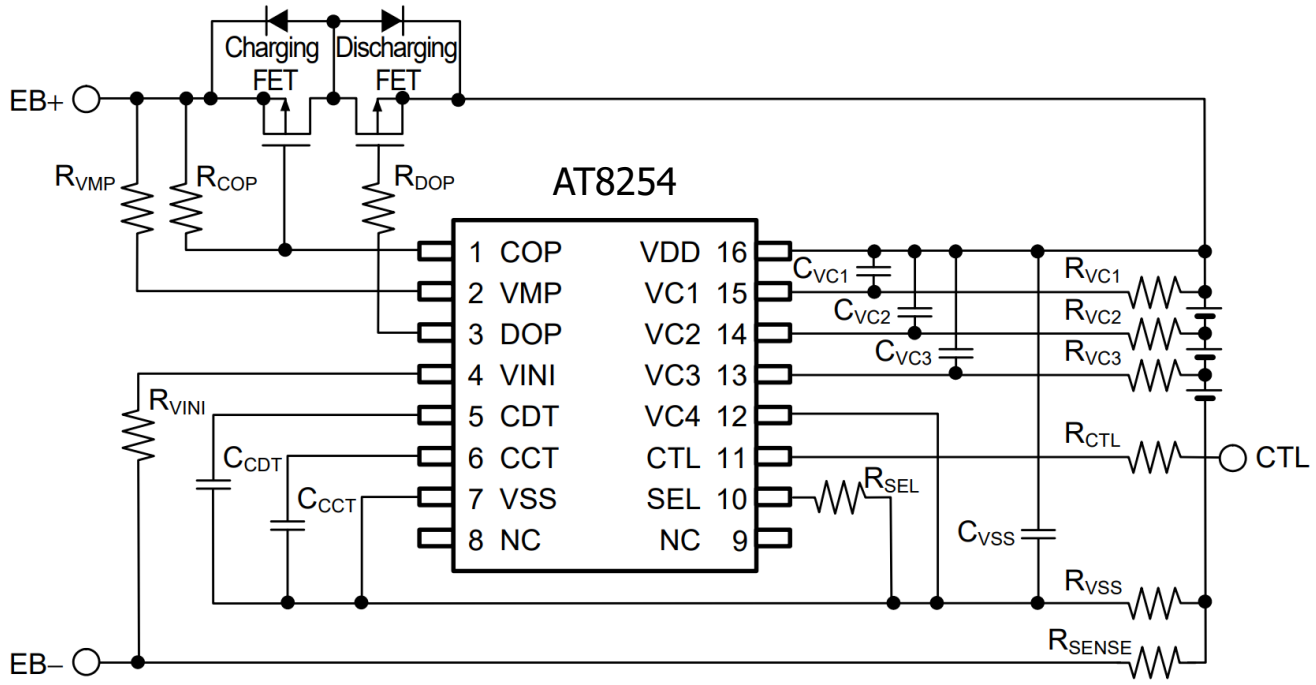


Figure 9.

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Constants for External Components

No.	Symbol	Min.	Typ.	Max.	Unit	No.	Symbol	Min.	Typ.	Max.	Unit
1	R_{VC1}	0	1	1	kΩ	11	R_{SENSE}	0	-	-	mΩ
2	R_{VC2}	0	1	1	kΩ	12	R_{VSS}	10	51	51	Ω
3	R_{VC3}	0	1	1	kΩ	13	C_{VC1}	0	0.1	0.33	μF
4	R_{VC4}	0	1	1	kΩ	14	C_{VC2}	0	0.1	0.33	μF
5	R_{DOP}	2	5.1	10	kΩ	15	R_{VC3}	0	0.1	0.33	μF
6	R_{COP}	0.1	1	1	MΩ	16	C_{VC4}	0	0.1	0.33	μF
7	R_{VMP}	1	5.1	10	kΩ	17	C_{CCT}	0.01	0.1	-	μF
8	R_{CTL}	0	0	100	kΩ	18	C_{CDT}	0.07	0.1	-	μF
9	R_{VINI}	0	1	100	kΩ	19	C_{VSS}	2.2	2.3	10	μF
10	R_{SEL}	0	0	100	kΩ						

Note: Please set up a filter constant to be

$R_{VSS} \times C_{VSS} \geq 51\ \mu F \bullet \Omega$,

and $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VC4} \times C_{VC4} = R_{VSS} \times C_{VSS}$.

Caution

1. The constants may be changed without notice.

2. It is recommended that filter constants between VDD and VSS should be set approximately to 112 μF • Ω.

e.g. CVSS × RVSS = 2.2 μF × 51 Ω = 112 μF • Ω

Enough evaluation of transient power supply variation and overcurrent protection function in the actual application is needed to determine the proper constants. Contact our sales representatives in case the constants should be set to other than 112 μF • Ω or so.

3. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

Precautions

• The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.

• Batteries can be connected in any order, however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VMP pin and VDD pin or connect the battery charger to return to the normal status.

• When an overcharged battery and an overdischarged battery intermix, the circuit is in both the overcharge and overdischarge statuses, so charging and discharging are not possible.

• Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

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TYPICAL CHARACTERISTICS

1. Current Consumption

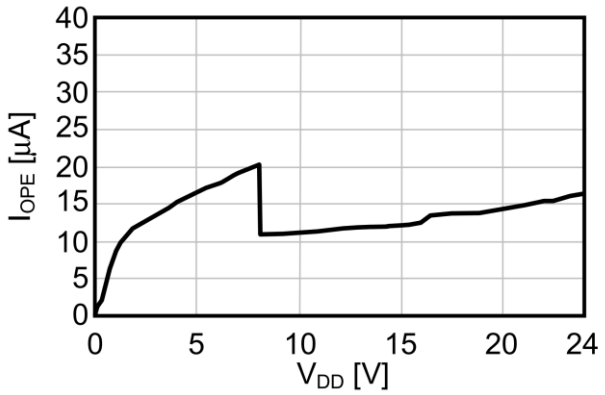


Figure 10. I_{OPE} vs. V_{DD}

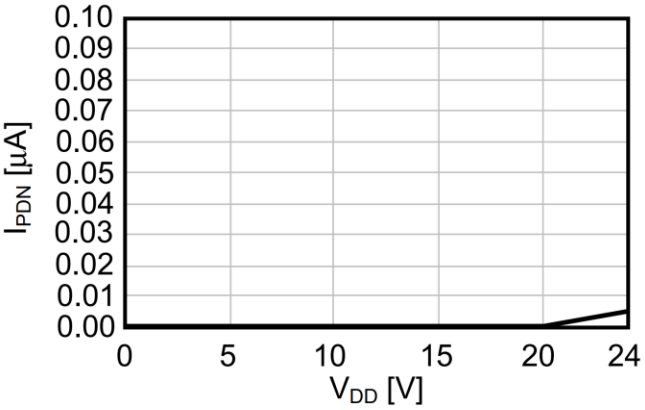


Figure 12. I_{PDN} vs. V_{DD}

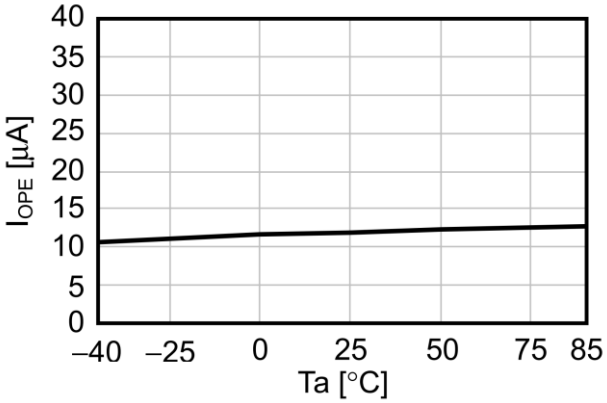


Figure 11. I_{OPE} vs. Ta

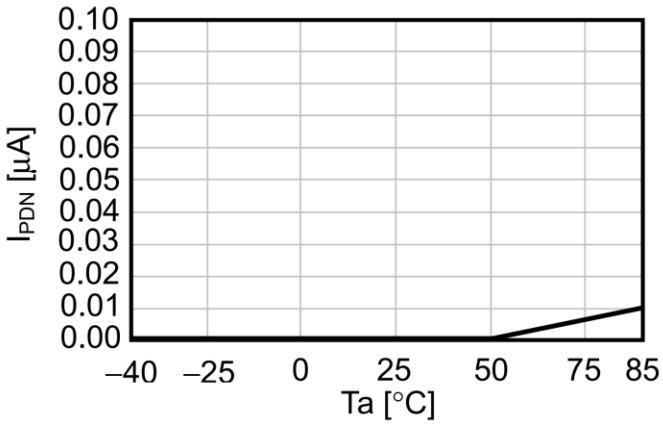


Figure 13. I_{PDN} vs. T

2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Overcurrent Detection Voltage, and Delay Times

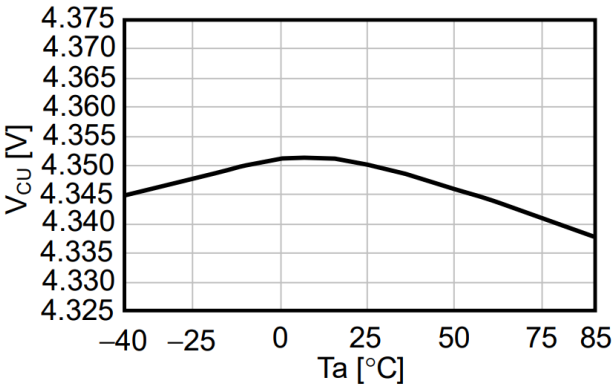


Figure 14. V_{CU} vs. Ta

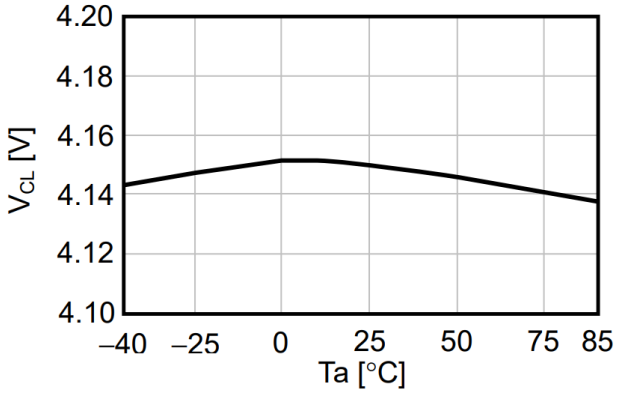


Figure 15. V_{CL} vs. Ta

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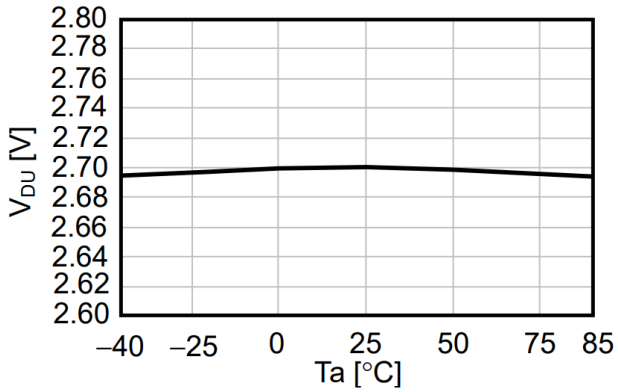


Figure 16. V_{DU} vs. Ta

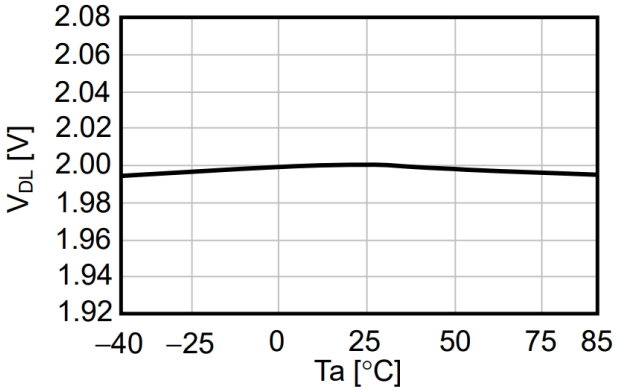


Figure 17. V_{DL} vs. Ta

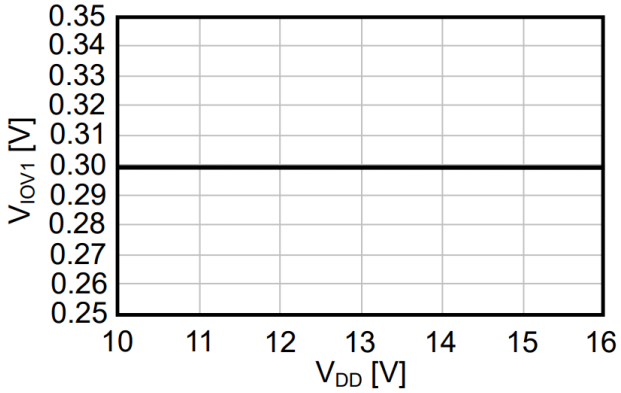


Figure 18. V_{IOV1} vs. V_{DD}

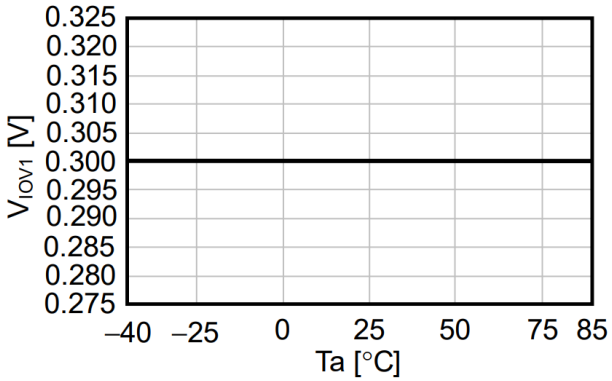


Figure 19. V_{IOV1} vs. Ta

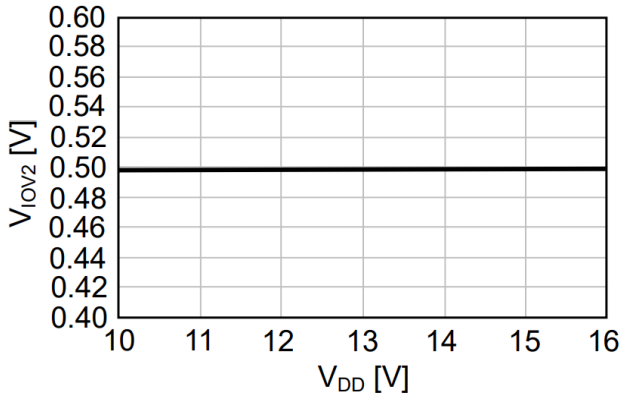


Figure 20. V_{IOV2} vs. V_{DD}

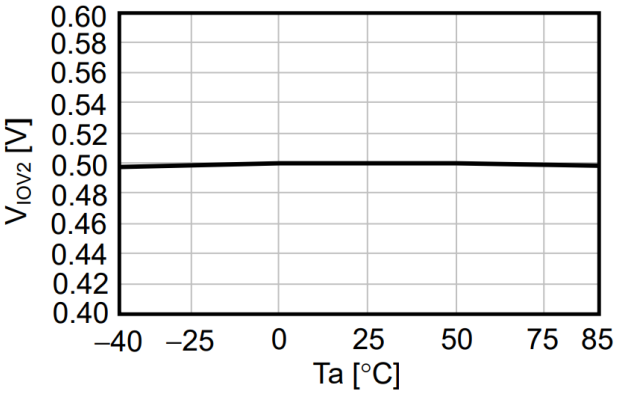


Figure 21. V_{IOV2} vs. Ta

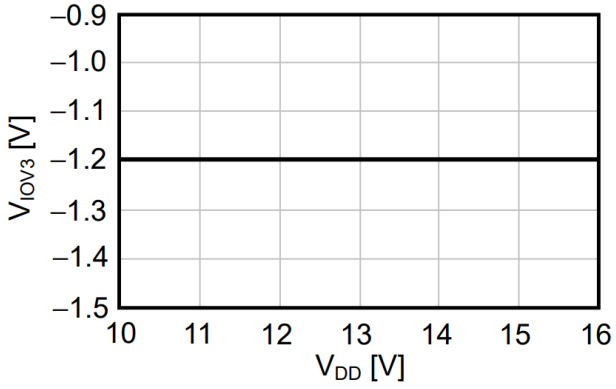


Figure 22. V_{IOV3} vs. V_{DD}

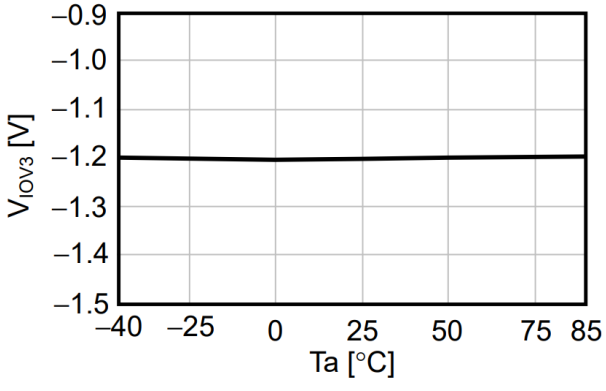


Figure 23. V_{IOV3} vs. Ta

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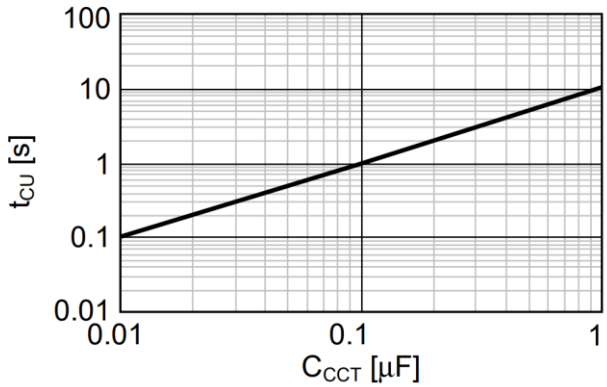


Figure 24. t_{CU} vs. C_{CCT}

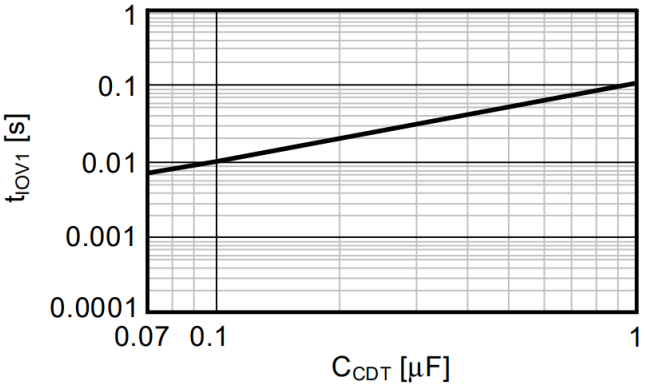


Figure 27. t_{IOV1} vs. C_{CDT}

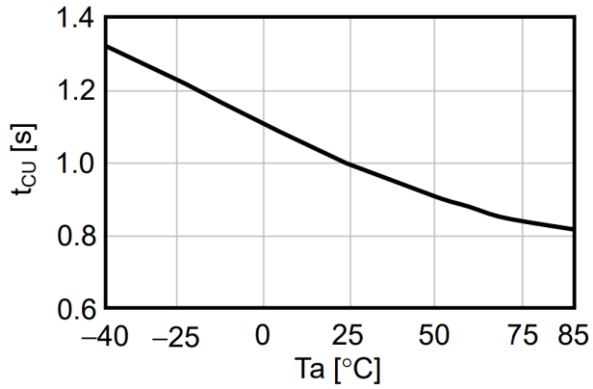


Figure 25. t_{CU} vs. Ta

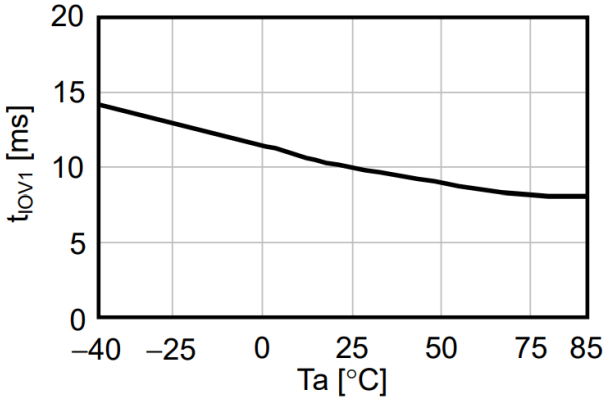


Figure 28. t_{IOV1} vs. Ta

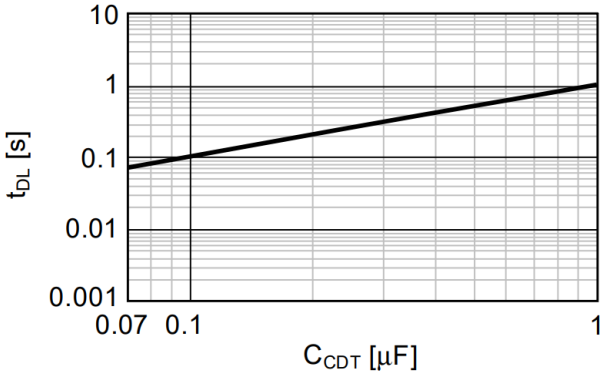


Figure 25. t_{DL} vs. C_{CDT}

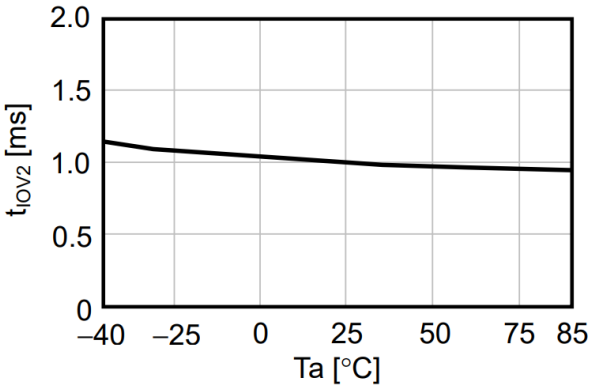


Figure 29. t_{IOV2} vs. Ta

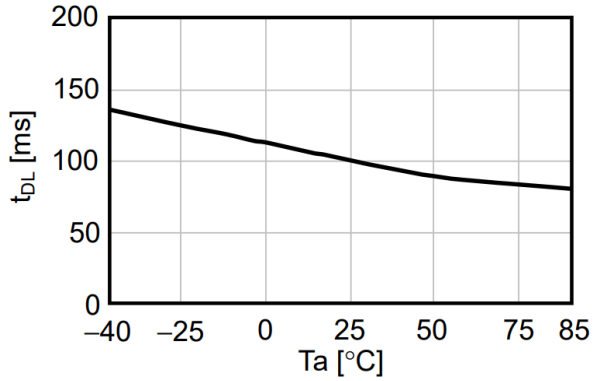


Figure 26. t_{DL} vs. Ta

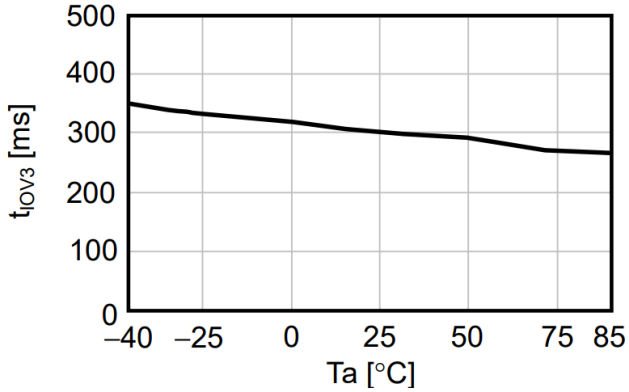


Figure 30. t_{IOV3} vs. Ta

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3. COP / DOP Pin

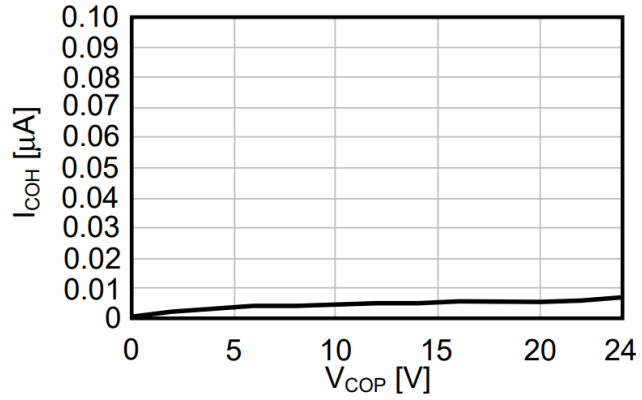


Figure 31. I_{COH} vs. V_{COP}

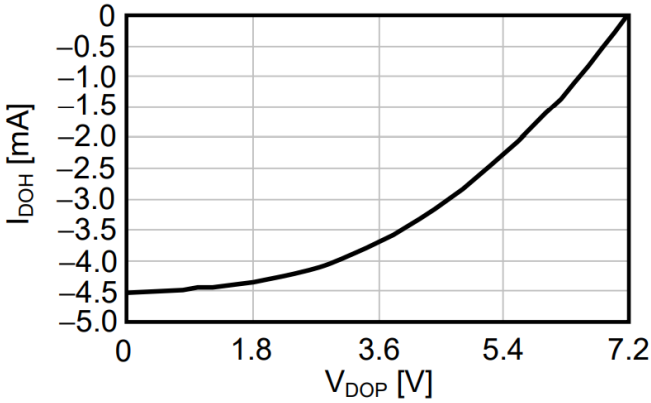


Figure 33. I_{DOH} vs. V_{DOP}

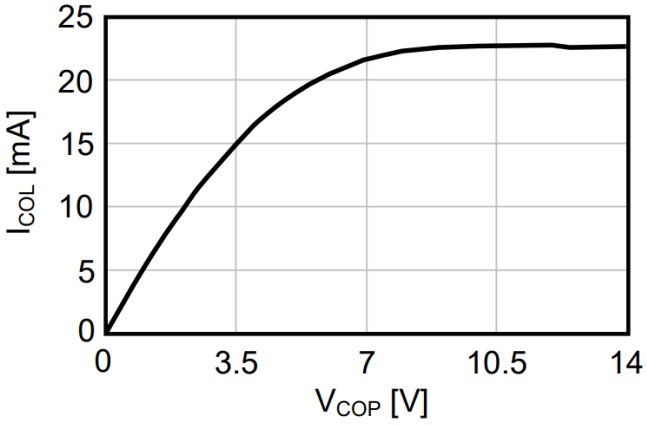


Figure 32. I_{COL} vs. V_{COP}

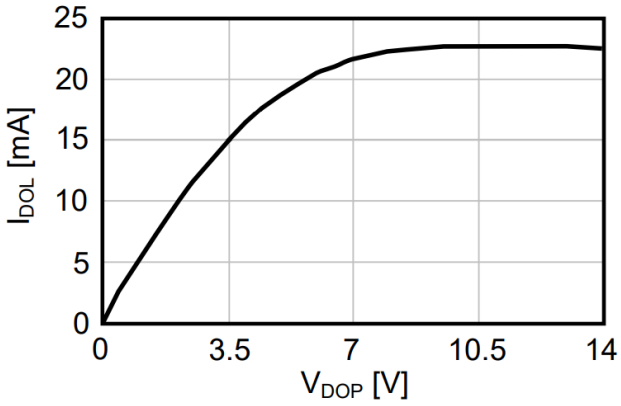


Figure 34. I_{DOL} vs. V_{DOP}

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OUTLINE DIMENSIONS

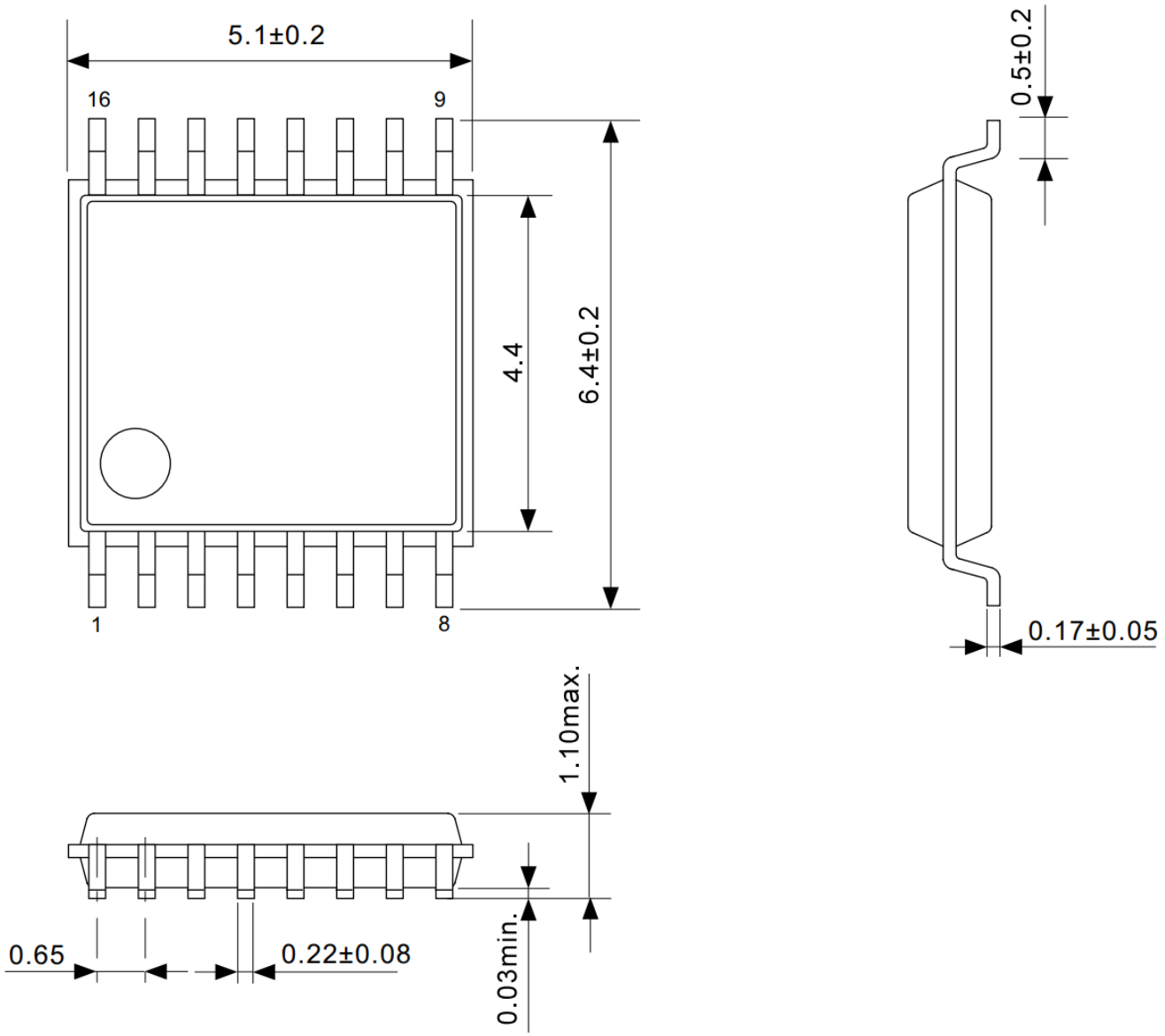


Figure 35. Outline Dimensions

ORDERING INFORMATION

Part Number	Buy Now
AT8254	

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