

Figure 1. Top View of AT6577

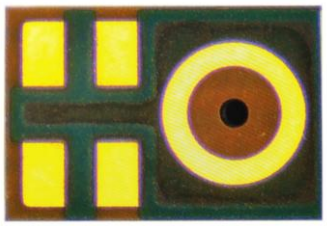


Figure 2. Bottom View of AT6577

ORDERING GUIDE

Online Stores		Commission Fee	Unit Price (June 2024)	Buy Now
AS	shop.analogtechnologies **Our own online store**	Zero sale commission	$0.84/100PCs	*
SZ	SMTZone **Our own online store**	Zero sale commission	$0.84/100PCs	*
K	Digikey	≈24% sale commission	$1.04/100PCs	*

FEATURES

- The lowest frequency microphone in the world
- Stable sensitivity over power supply range of 1.6V~3.6V
- SNR of 64dB(A)
- Sensitivity of −26dB FS
- Dual Mode Operation: Active Mode and Low-Power Sleep Mode
- Multi Chip Module (MCM) Package
- 2.75mm×1.85mm×0.9mm surface-mount package

APPLICATIONS

- Mobile Telephones
- PDAs
- Digital Video Cameras
- Portable Media Devices with Audio Input

DESCRIPTION

The AT6577 is a high quality, low cost, low power digital output bottom-ported omni-directional MEMS microphone. AT6577 consists of a MEMS microphone element and a preamplifier. AT6577 has a high SNR and flat wideband frequency response, resulting in natural sound with high intelligibility. Due to built-in filter, AT6577 shows high immunity to EMI.

The AT6577 supports dual-mode operation controlled by the external clock input.

Active Mode: when a valid clock signal is applied to the CLK pin, the AT6577 operates in Active Mode.

In this mode:

- The device outputs PDM digital audio data
- Full acoustic performance is enabled
- Sensitivity and SNR meet specified electrical characteristics

Low-Power Sleep Mode

When the clock frequency is reduced or removed, the device enters Low-Power (Sleep) Mode.

In this mode:

- PDM data output is disabled or invalid
- Internal circuitry is partially powered down
- Current consumption is significantly reduced
- When the clock is fully removed, the device automatically enters Power-Down state

The AT6577 is available in a thin 2.75mm × 1.85mm

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× 0.90mm surface-mount package. It is reflowing solder compatible with no sensitivity degradation. The AT6577 is Halogen and Lead free.

PIN CONFIGURATIONS

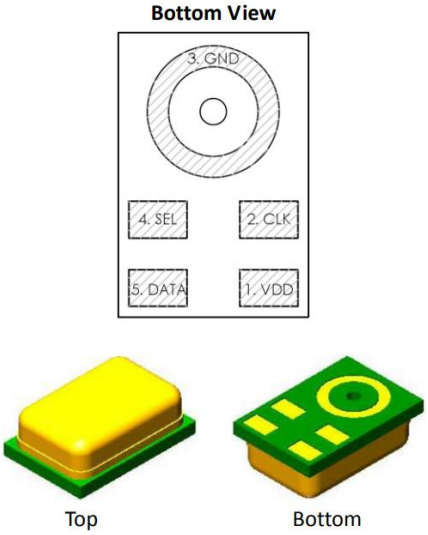


Figure 3. Pin Configurations

PIN DESCRIPTION

Table 1.

Pin	Symbol	Description
1	VDD	Power supply
2	CLK	Clock
3	GND	Ground
4	SEL	Select
5	DATA	Output

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
CLOCK to Ground	−0.3V to +6.0V
SELECT, V_{DD}, DATA to Ground	−0.3V to +6.0V
Input Current	±5mA
Operating Temperature	−40°C to +125°C
Storage Temperature	−40°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

ESD CAUTION

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with proper precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

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ELECTRICAL CHARACTERISTICS

(T_A = +15°C ~ +25°C, V_{DD} = +1.8V, f_{clock} = 3.072MHz, R.H. = 60%~70%, no load, unless otherwise noted.)

Table 3.

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Power Supply Voltage[1]	V_{DD}			1.6		3.6	V
Clock Frequency	f_{clock}			1.0		4.8	MHz
Current Consumption t[1,6]	I_{DD}				600	700	μA
Standby Current (Sleep Mode) [5, 6]	$I_{STANDBY}$	f_{clock} < 250kHz			50		μA
Directivity				Omni-directional			
Sensitivity[1]	S	94dB SPL @1kHz		−27	−26	−25	dB FS
Signal to Noise Ratio	SNR	94dB SPL @1kHz, A-weighted			64		dB(A)
Total Harmonic Distortion	THD	114dB SPL 1 kHz				1	%
		120dB SPL 1 kHz				10	%
Acoustic Over load Point	AOP	10% THD @1kHz			120		dB SPL
Power Supply Rejection Ratio	PSRR	1kHz, 200mV_{p-p}, square wave on V_{DD}	V_{DD}= 1.8V		60		dB
			V_{DD}= 3.3V		60		
Power Supply Rejection	PSR	217Hz, 100mV_{p-p}, square wave on V_{DD}	V_{DD}= 1.8V		−90		dB FS
			V_{DD}= 3.3V		−90		
Polarity		Increasing sound pressure		Increasing density of 1's			
Fall-Asleep Time[2, 3]		V_{DD} = On, f_{clock} < 1KHz				10	ms
Wake-Up Time[2, 4]		V_{DD} = On, f_{clock} ≥ 1KHz				10	ms
Short Circuit Output Current	I_{SC}	Grounded output pin			1	10	mA
Output Load	C_{LOAD}					100	pF
Data Format				1/2 cycle PDM			
Clock Duty Cycle				40		60	%
Clock Rise Time	t_{cr}					10	ns
Clock Fall Time	t_{ct}					10	ns
Logic Input/Output Low	V_{IOL}	I_{out} = 1mA		−0.3		0.35×V_{DD}	V

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Parameter	Symbol	Test Conditions			Min.	Typ.	Max.	Unit
Logic Input/Output High	V_{IOH}	I_{out} = 1mA			0.65×V_{DD}		V_{DD}+0.3	V
Delay Time for Valid Data	t_{dv}	CLK = 3.072MHz, Oscilloscope: APx525 (probe Cin = 24pF)	Data Transition High	1.8V	26		82	ns
				3.3V	20		80	
			Data Transition Low	1.8V	25		80	
				3.3V	21		81	
Delay Time for High Z	t_{dz}	CLK = 3.072MHz, Oscilloscope: APx525 (probe Cin = 24pF)	Data Transition High	1.8V	0		25	ns
				3.3V	0		24	
			Data Transition Low	1.8V	0		26	
				3.3V	0		25	
Settling time	t_s			1.8V		2.65	5.5	ms
				3.3V				
Startup Time		Powered Down →Active Mode		1.8V		2.65	5.5	ms
				3.3V		2.45	5.3	

(T_A = +15°C ~+25°C, V_{DD} = 3.3V, f_{clock} = 768KHz, R.H. = 60%~70%, no load, unless otherwise noted.)

Table 4.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage[1]	V_{DD}		1.6		3.6	V
Clock Frequency	f_{clock}		350		800	kHz
Current Consumption t[1,6]	I_{DD}			260	300	μA
Standby Current (Sleep Mode) [5, 6]	$I_{STANDBY}$	f_{clock} < 250kHz		50		μA
Directivity			Omni-directional			
Sensitivity[1]	S	94dB SPL @1kHz	−27	−26	−25	dB FS
Signal to Noise Ratio	SNR	94dB SPL @1kHz, A-weighted		64		dB(A)
Total Harmonic Distortion	THD	114dB SPL 1 kHz			1	%
		120dB SPL 1 kHz			10	%
Acoustic Over load Point	AOP	10% THD @1kHz		120		dB SPL

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Parameter	Symbol	Test Conditions			Min.	Typ.	Max.	Unit
Power Supply Rejection Ratio	PSRR	1kHz, 200mV$_{p-p}$, square wave on V_{DD}	V_{DD}= 1.8V			60		dB
			V_{DD}= 3.3V			60		
Power Supply Rejection	PSR	217Hz, 100mV$_{p-p}$, square wave on V_{DD}	V_{DD}= 1.8V			−90		dB FS
			V_{DD}= 3.3V			−90		
Polarity		Increasing sound pressure			Increasing density of 1's			
Fall-Asleep Time[2, 3]		V_{DD} = On, f_{clock} < 1KHz					10	ms
Wake-Up Time[2, 4]		V_{DD} = On, f_{clock} ≥ 1KHz					10	ms
Short Circuit Output Current	I_{SC}	Grounded output pin				1	10	mA
Output Load	C_{LOAD}						100	pF
Data Format					1/2 cycle PDM			
Clock Duty Cycle					40		60	%
Clock Rise Time	t_{cr}						10	ns
Clock Fall Time	t_{ct}						10	ns
Logic Input/Output Low	V_{IOL}	I_{out} = 1mA			−0.3		0.35×V_{DD}	V
Logic Input/Output High	V_{IOH}	I_{out} = 1mA			0.65×V_{DD}		V_{DD}+0.3	V
Delay Time for Valid Data	t_{dv}	CLK = 3.072MHz, Oscilloscope: APx525 (probe Cin = 24pF)	Data Transition High	1.8V	26		82	ns
				3.3V	20		80	
			Data Transition Low	1.8V	25		80	
				3.3V	21		81	
Delay Time for High Z	t_{dz}	CLK = 3.072MHz, Oscilloscope: APx525 (probe Cin = 24pF)	Data Transition High	1.8V	0		25	ns
				3.3V	0		24	
			Data Transition Low	1.8V	0		26	
				3.3V	0		25	
Settling time	t_s			1.8V		2.65	5.5	ms
				3.3V				
Startup Time		Powered Down		1.8V		2.65	5.5	ms

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Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
		→Active Mode	3.3V		2.45	5.3	

Note 1: 100% tested.

Note 2: Valid microphone states are: Power Down Mode (mic off), Sleep Mode (low current, no output, fast start-up), and Active Mode (normal operation).

Note 3: Time from fclock < 1KHz to sleep current specification is met when transitioning from Active to Sleep Mode.

Note 4: Time from fclock ≥ 1MHz to all applicable specifications when transitioning from Sleep to Active Mode.

Note 5: $\Delta I_{DD} = 0.5 \times V_{DD} \times C_{LOAD} \times f_{clock}$

Note 6: Specified max values are measured at V_{DD} = +3.6V.

BLOCK DIAGRAM

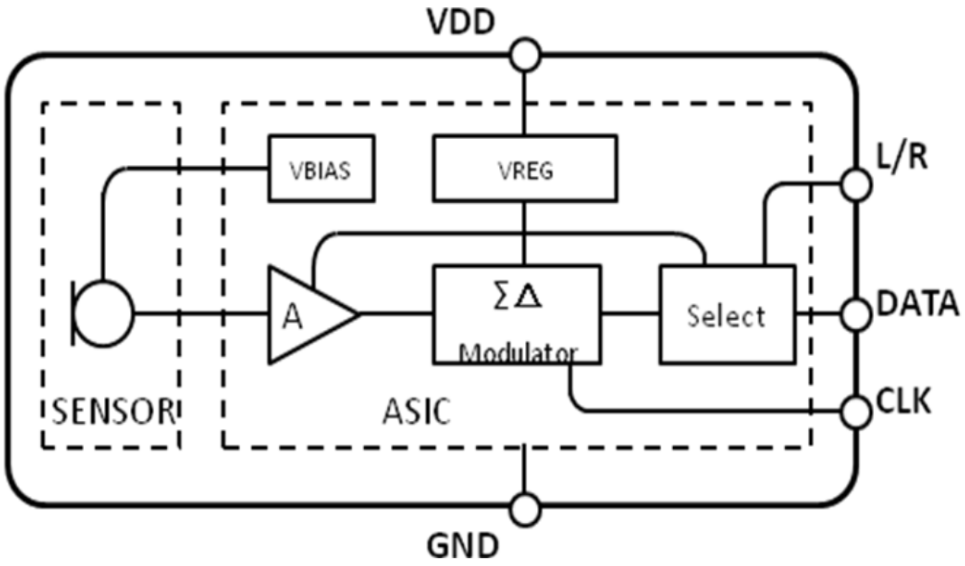


Figure 4. Block Diagram

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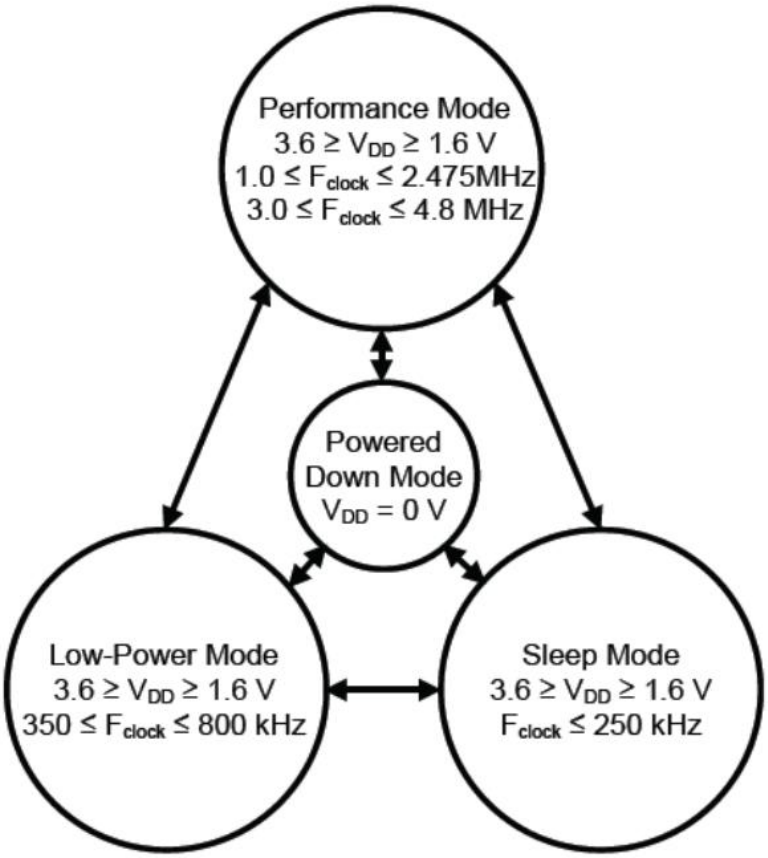


Figure 5. State Diagram

TYPICAL CIRCUIT APPLICATION

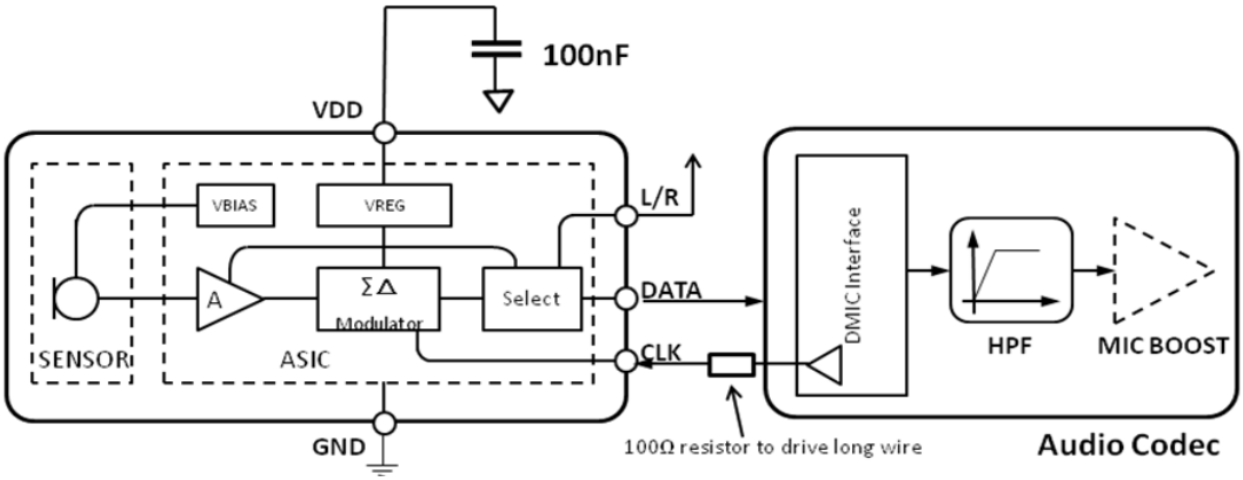
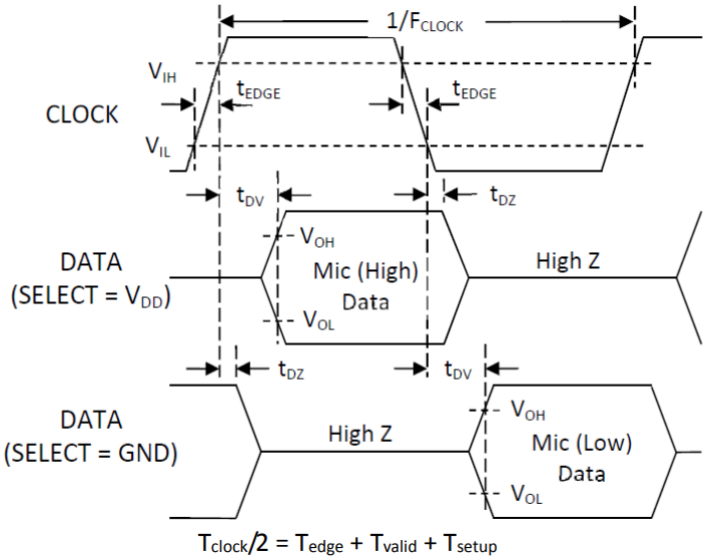


Figure 6. Typical Circuit

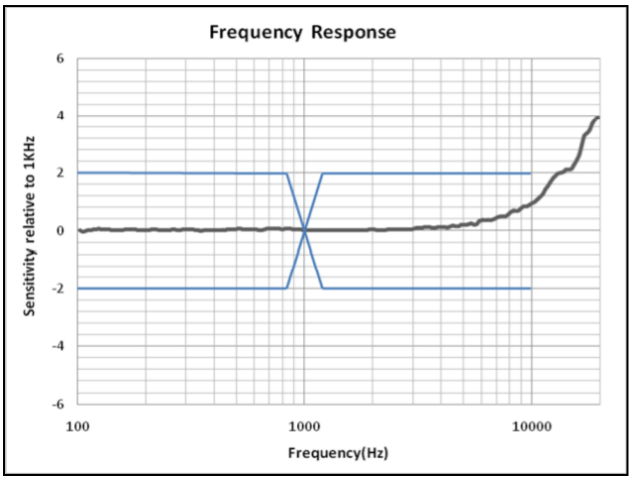
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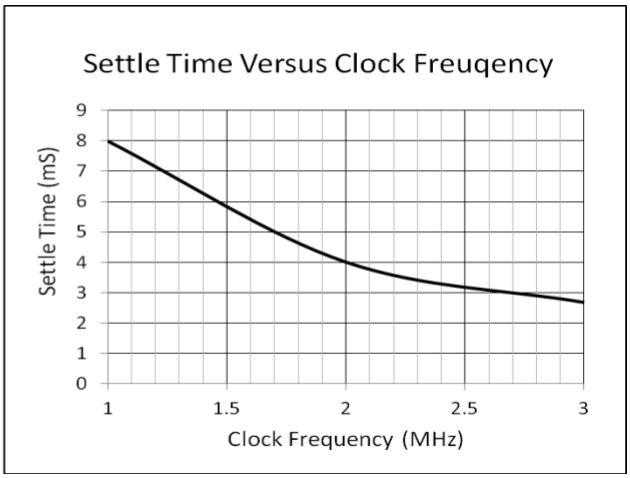
TIMING DIAGRAM

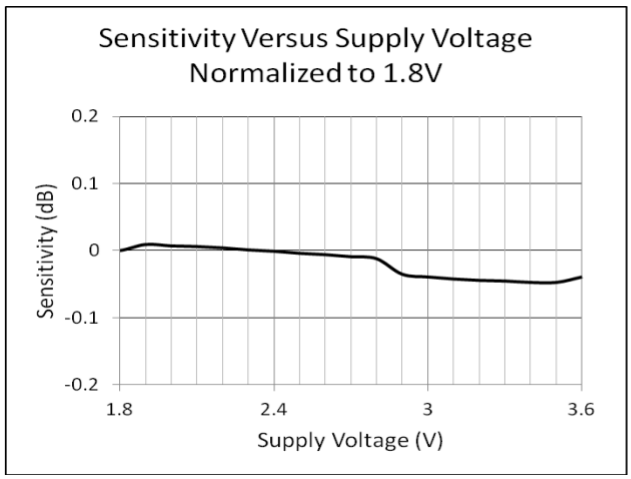


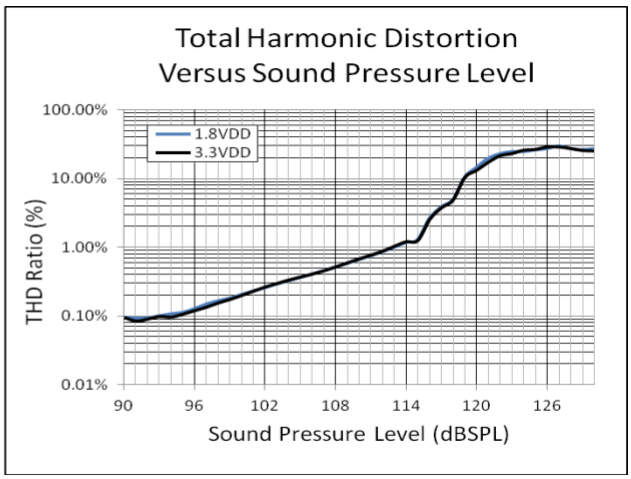
$T_{clock}/2 = T_{edge} + T_{valid} + T_{setup}$

TYPICAL CHARACTERISTICS

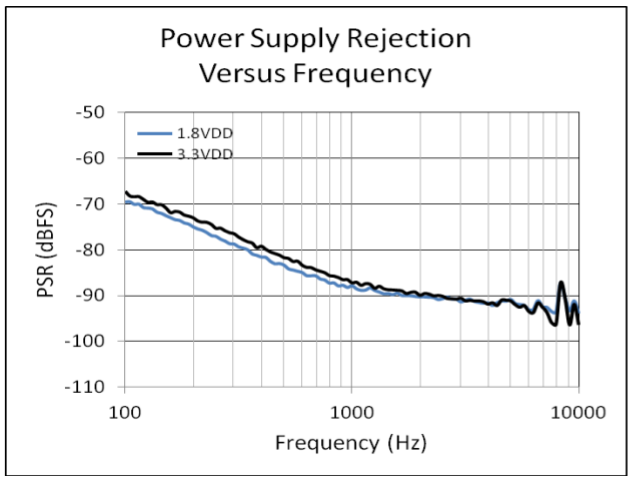


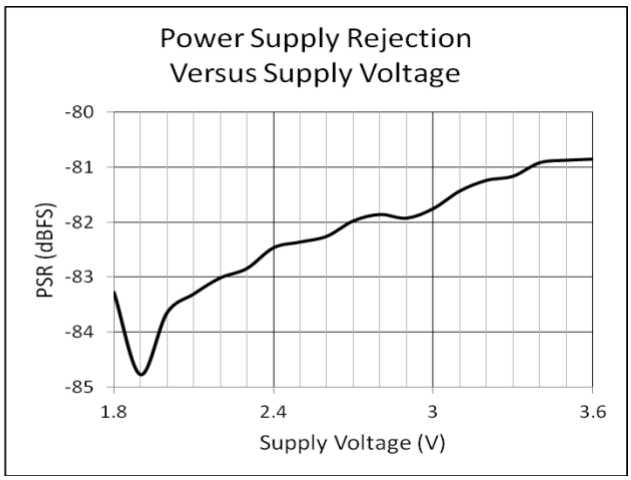






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RELIABILITY SPECIFICATIONS

The microphone sensitivity after stress must deviate by no more than ±3dB from the initial value.

1. Heat Test, Operational	Temperature: 125±3°C Duration: 1000 hours Voltage: Applied
2. Cold Test, Operational	Temperature: −40±3°C Duration: 1000 hours Voltage: Applied
3. Heat Test, Non-Operational	Temperature: 125±3°C Duration: 1000 hours Voltage: Not Applied
4. Cold Test, Non-Operational	Temperature: −40±3oC Duration:1000 hours Voltage: Not Applied
5. Thermal Shock Test, Non-Operational	Temperature: −40±3°C and 125±3°C Duration: 30 minutes each, during 5 minutes ramp, 256 cycles Voltage: Not applied
6. Temperature humidity storage	Temperature: 85±3°C Humidity: 85±3%RH Duration: 1000 hours
	Temperature: 65±3°C Humidity: 95±3%RH Duration: 168 hours
7. Free Fall Test 1.5m	Placed inside test fixture and dropped on concrete from height 1.5m. 4 times by each surface and corner.
8. Vibration	4 cycles of 20 to 2000 Hz sinusoidal sweep with 20G peak acceleration lasting 12 minutes in X, Y, and Z directions.
9. Mechanical Shock	5 pulses of 10000g in each of the ±X, ±Y, and±Z directions.

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10. Electrostatic Discharge Test	Capacitance: 150pF Resistance: 330Ω Duration: 10 times Air Discharge: Level 4 (±15kV) Direct contact discharge: Level 4 (±8kV)
11. Human Body Mode	±2000 Volt
12. Charged-Device Model	±250 Volt
13. Reflow	5 reflow cycles with peak temperature of 260°C
14. Solderability	245±5°C, 5sec, 95% Tin on pad surface
15. Tumble test	300 tumbles from a height of 1m onto a steel base.
16. HAST	Temperature: 130±3°C Humidity: 85±3%RH Duration: 96 hours Voltage: Applied
17. Air Blow	0.45MPa, distance: 3cm, time: 10s

OUTLINE DIMENSIONS

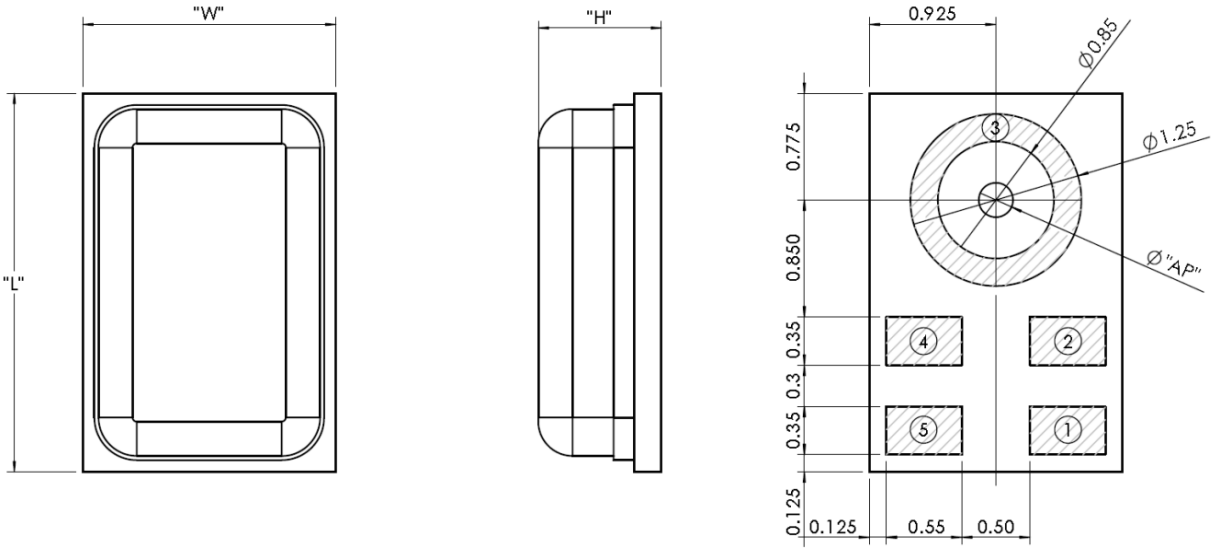


Figure 7. Outline Dimensions

Symbol	Dimensions		Tolerance	
	mm	inch	mm	inch
Length (L)	2.75	0.108	±0.100	±0.0039
Width (W)	1.85	0.073	±0.100	±0.0039
Height (H)	0.90	0.035	±0.100	±0.0039
Acoustic Port (AP)	0.25	0.010	±0.050	±0.0019

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RECOMMENDED CUSTOMER LAND PATTERN

The recommended PCB land pattern for the AT6577 should have a 1:1 ratio to the solder pads on the microphone package. Care should be taken to avoid applying solder paste to the sound hole in PCB. The dimensions of suggested solder paste pattern refer to the land pattern.

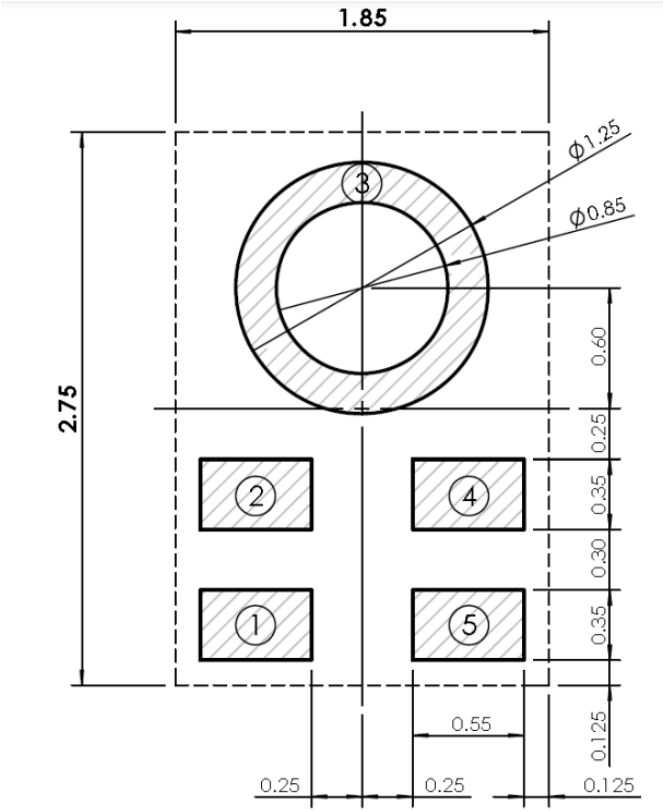
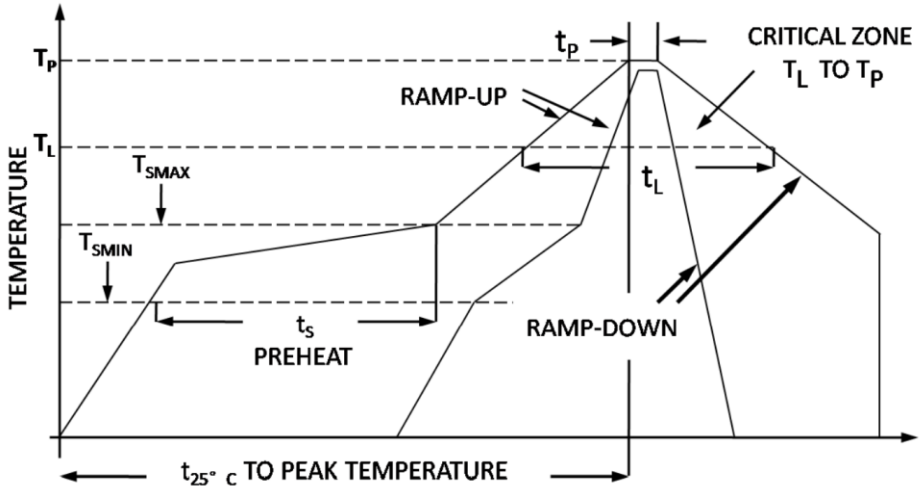


Figure 8. Recommended Land Pattern

SOLDER FLOW PROFILE

The reflow profile specified in this section describes expected maximum heat exposure of components during the reflow process of NMP product PWBs. Temperature is measured on top of component. All components have to tolerate at least this profile five times (5x) without affecting electrical performance, mechanical performance or reliability.



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Pb-free and Sn63/Pb37 reflow profile requirements for soldering heat resistance:

Parameter		Reference	Pb-Free	Sn63/Pb37
Average Ramp Rate		T_L to T_P	1.25°C/sec max	1.25°C/sec max
Prehear	Minimum Temperature	T_{SMIN}	100°C	100°C
	Maximum Temperature	T_{SMAX}	200°C	150°C
	Time	T_{SMIN} to T_{SMAX}	60sec to 120sec	60sec to 120sec
Ramp-Up Rate		T_{SMAX} to T_L	1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous		t_L	60sec to 150sec	60sec to 150sec
Liquidous Temperature		T_L	217°C	183°C
Peak Temperature		T_P	260°C +0°C/−5°C	215°C ±3°C
Time within +5°C of Actual Peak Temperature		t_P	20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate		Tpeak	6°C/sec max	6°C/sec max
Time +25°C ($t_{25°C}$) to Peak Temperature			8 min max	6 min max

ORDERING INFORMATION

Part Number	Buy Now
AT6577	

NOTICE

1. It is important to carefully read and follow the warnings, cautions, and product-specific notes provided with electronic components. These instructions are designed to ensure the safe and proper use of the component and to prevent damage to the component or surrounding equipment. Failure to follow these instructions could result in malfunction or failure of the component, damage to surrounding equipment, or even injury or harm to individuals. Always take the necessary precautions and seek professional assistance if unsure about proper use or handling of electronic components.
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10. Despite operating the electronic modules as specified, malfunctions or failures may occur before the end of their usual service life due to the current state of technology. Therefore, it is crucial for customer applications that require a high level of operational safety, especially in accident prevention or life-saving systems where the malfunction or failure of electronic modules could pose a risk to human life or health, to ensure that suitable measures are taken. The customer should design their application or implement protective circuitry or redundancy to prevent injury or damage to third parties in the event of an electronic module malfunction or failure.

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