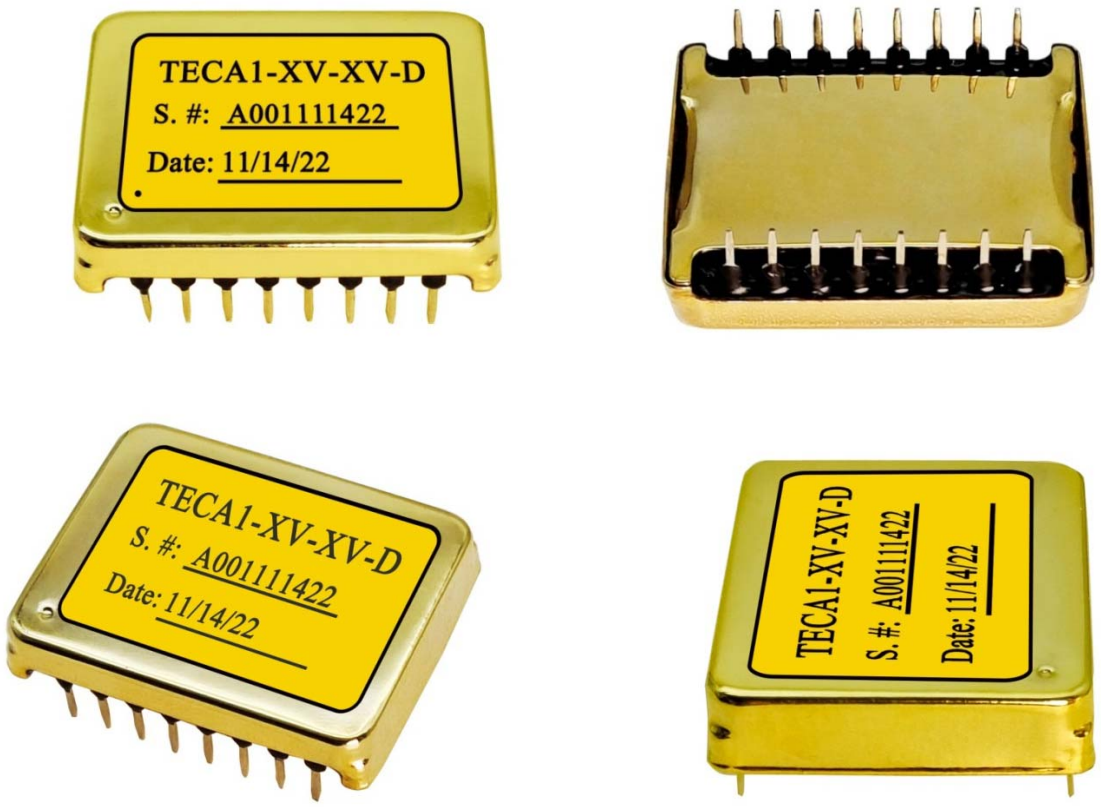


Figure 1. The Gold Module TEC Controller

FEATURES

- High Efficiency: ≥90%
- I_{OUTMAX}: 2.5A
- Target Object Temperature Monitor
- High Temperature Stability: 0.01°C
- Vacuum potted and low outgassing
- Gold Plated for High Reliability and Zero EMI
- Compact Size
- 100% lead (Pb)-free and RoHS compliant

DESCRIPTION

The TECA1-XV-XV-D is a compact gold plated electronic module designed for driving TECs (Thermo-Electric Coolers) with minimum external components to achieve high temperature stability high energy efficiency, and zero EMIs. It is vacuum potted thus also suitable for space applications.

Warning: This controller module can only be soldered manually onto the board by a solder iron at < 310°C (590°F), it cannot go through a reflow oven process.

INTERFACING WITH DIGITAL PERIFERALS

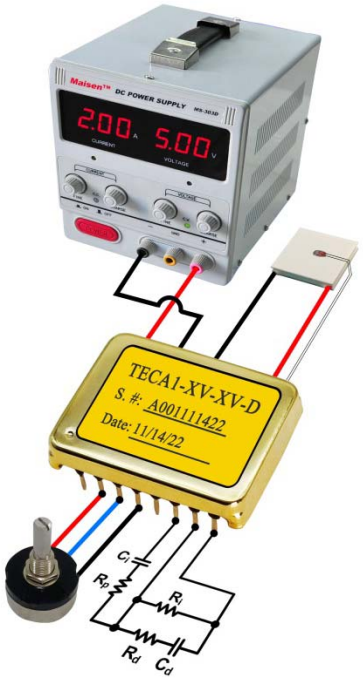


Figure 2. 3D Figure

Figure 3 is the real size top view of the controller showing the pin names and locations. The functions of all the pins are described in Table 1.

The TECA1-XV-XV-D is packaged in a 6-sided metal enclosure, which blocks EMIs (Electro-Magnetic Interferences) to prevent the controller and other electronics from interfering with each other.

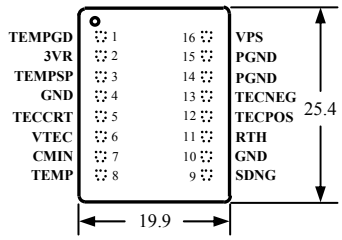


Figure 3. Pin names and Locations

The compensation network for the thermal control loop is consisted 5 components: 3 resistors and 2 capacitors. This network can be implemented either internally by embedding them inside the controller enclosure or externally by soldering the 5 components onto the PCB (Printed Circuit Board) on which the TEC controller is mounted. The latter is highly recommended since it can be modified for driving different thermal loads and/or the thermal load characteristics may not be certain or fixed at the early design stage.

The TEC controller can be ordered with or without an internal compensation network. The part number TECA1LD-XV-XV-D, *with* the "LD" suffix, stands for the controller *with* an internal compensation network with the default values shown in Figure 10 which matches the TEC thermal load found in the ubiquitous butter-fly packaged lasers.; while the part number TECA1-XV-XV-D, *without* the "LD" suffix, stands for the controller *without* the internal compensation network and an external compensation network will be required for the controller to operate.

Controller part number naming: the first "X" in the part number, TECA1-XV-XV-D, denotes the input power supply voltage, it can be "5" for 5V and "3" for 3V. The 2nd "X" denotes the maximum output voltage, the possible values include: "5" for 5V, "3" for 3V, "2.5" for 2.5V, "2" for 2V, etc. More details for naming is given in Table 3 below.

BLOCK DIAGRAM

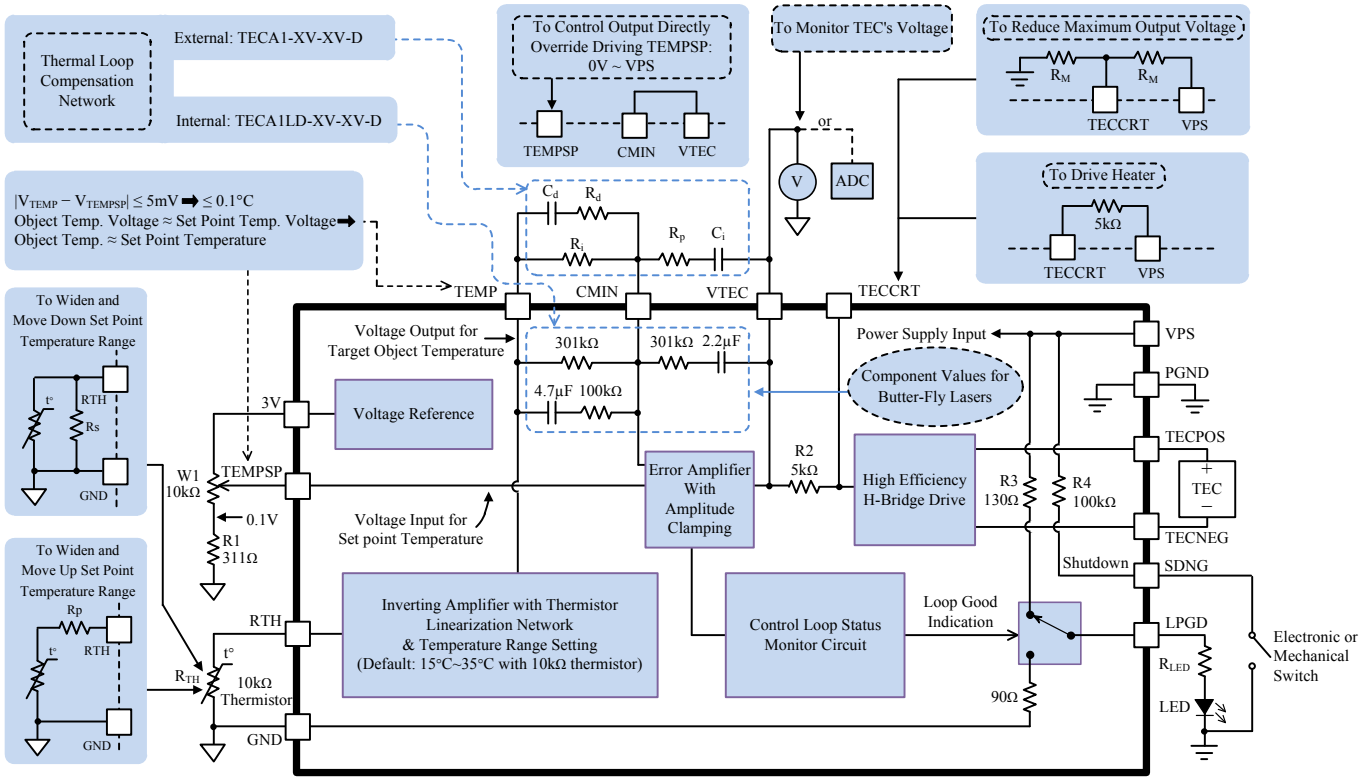


Figure 4. TEC Controller Functional Block Diagram

WORKING PRINCIPL

Input Thermistor Amplifier

At the input of the controller, there is a polarity inverting amplifier with a thermistor linearization network. It converts the thermistor's non-linear negative relationship of temperature vs. resistance into a linear positive relationship of temperature vs. a voltage at the output, TEMP, which represents the target object's actual temperature.

Error Amplifier for Thermal Loop

The TEMP voltage is sent to an error amplifier to compare with a voltage representing the set-point temperature in order to generate a control voltage at VTEC as the control signal for the output stage. Before reaching the output stage, a 5kΩ resistor is inserted, resulting in the TECCRT node. It allows adding external resistors to reduce the maximum output voltage applied to the TEC or change the bipolar output into a unipolar type for driving heaters.

Compensation Network for Thermal Loop

Since the TEC thermal load is a second order plant, driving it directly will cause the close loop oscillate. There compensation network shifts and sets the close loop poles and zeros thus the loop be stable and respond to the change for set-point temperature, thermal load active power, and/or ambient temperature with a short rise and fall times and minimum setting period. Thus the target object temperature will always as close be the same as the set-point temperature.

Loop Good Detection Circuit

There is a control loop monitor circuit. When seeing the controller works properly and the target object actual temperature is within 0.1°C away from the set-point temperature, the circuit pulls the TEMPGD pin high by a 130Ω resistor to the VPS power rail, otherwise, including shut down state, it is pulled down by a 90Ω resistor to the ground.

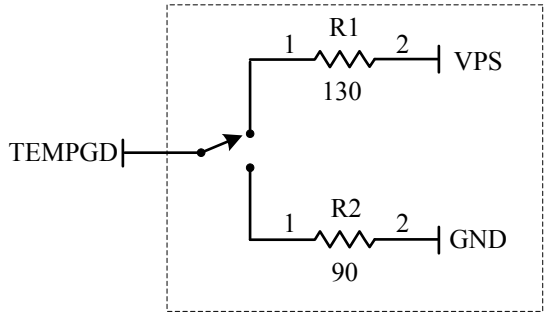


Figure 5. Internal Equivalent Circuit on TEMPGD Pin

Reference Voltage

The TECA1-XV-XV-D comes with a high stability low noise 3.0V voltage reference, which can be used for setting the desired target object's temperature by using a POT (Potentiometer) or a DAC (Digital to Analog Converter). When using this reference for setting the set-point temperature port, TEMPSP, the change in the reference voltage won't cause any set-point temperature errors, inspite of the change on the TEMPSP pin caused by the reference. This is because internal temperature measurement network also uses this voltage as the reference, the errors in setting the temperature and measuring the temperature cancel with

Override Internal Voltage Setting

When the controller does not connect anything externally, the V_{TEMPSP} is 1.5V. If the controller connects a DAC or Potentiometer externally, remove the two 100kΩ resistors in the circuit in Figure 6. Please note that these two resistors are 10MΩ before June 26, 2022, and will be changed to 100kΩ after this date.

For applications that do not need the internal resistors in Figure 6, the part number becomes TECA1-XV-XV-D-OP.

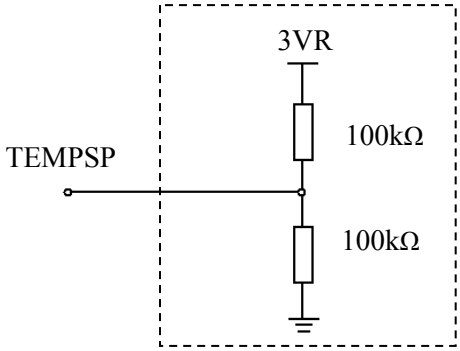


Figure 6. Internal Equivalent Circuit on TEMPSP Pin

Quiescent Current VS. Shutdown Voltage

Figure 7 shows how the quiescent current (I_Q) changes with the voltage of Pin SDNG (V_{SDNG}).

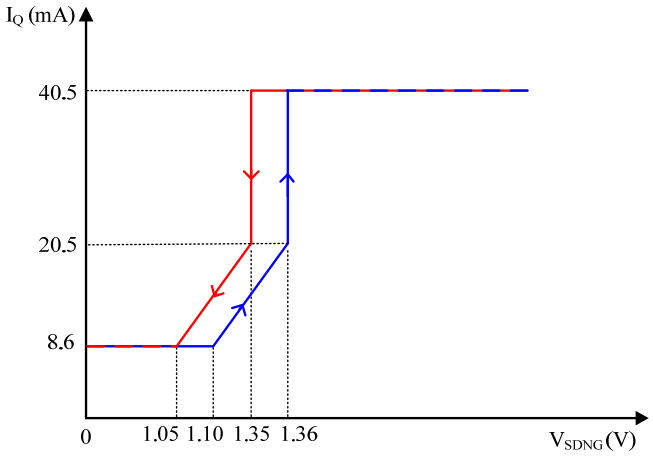
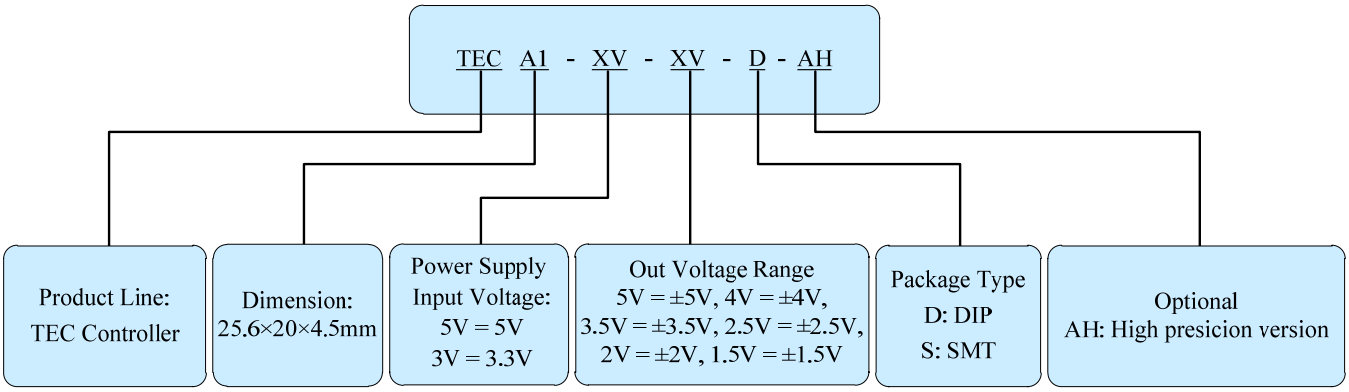


Figure 7. I_Q vs. V_{SDNG}

NAMING



Naming Principle of TECA1-XV-XV-D

SPECIFICATIONS

Table 1. Pin Function Descriptions

Pin #	Pin Name	Type	Description
1	**TEMPGD**	Digital output	This pin is pulled up to the VPS pin by a 130Ω resistor when the controller is working and the target object temperature is within <0.1°C away from equals the set-point temperature value or within <5mV difference between the voltages on TEMP and TEMPSP pins, otherwise it is pulled down by a 90Ω resistor to the GND pin. It can be used to drive an LED as an indication that the controller works properly and thermal loop is stabilized.
2	**3VR**	Analog output	This pin outputs a 3V low noise highly stable reference voltage. It can be used by a POT or DAC for setting the set-point temperature voltage on the TEMPSP pin and/or a DAC for measuring the temperature on the TEMP pin. The maximum sourcing current capability is 1.5mA and the maximum sinking is 4mA with a stability of <50ppm/°C max.
3	**TEMPSP**	Analog input	This pin sets the target object temperature from 0.1V to 3V corresponding to a temperature range from 15°C to 35°C linearly. It is internally connected to 1.5V by a 50kΩ resistor, thus, leaving this pin unconnected results in 1.5V setting voltage and corresponding to 25C in temperature. It is highly recommended to set this pin's voltage by using the controller's built-in 3V voltage reference. The lower limit for setting this pin is 0.1V. Setting this pin to a <0.1V voltage may cause the controller over cooling the object because the TEMP port cannot output a voltage <0.1V. This pin can also be set to a voltage 0.2V below VPS rail. When V_{VPS} = 5V, setting this pin to 4.8V corresponds to approximately 50°C in temperature when the default temperature network is in place, see the curve shown in Figure 20. This pin can be set by using a POT or DAC.
4	**GND**	Ground	Signal ground for the POT, ADC, DAC and the thermistor, see Figure 10.
5	**TECCRT**	Both analog input and output	TEC control voltage. It can be left unconnected or used to control the TEC voltage directly. Set TECCRT between 0V to V_{VPS}, the voltage across TEC will be: TEC voltage = $V_{VPS} - 2\times V_{TECCRT}$. It can also be used to configure the maximum voltage cross the TEC: Max. TEC voltage = $V_{TECmax} \times Rm / (Rm+10k)$, where V_{TECmax} is the maximum output voltage of the TEC controller configured by the internal limiting circuit when the controller is released by the factory, it is marked on the TEC controller label; Rm is the resistance of the two resistors one between TECCRT to GND and the other between TECCRT to VPS, as shown in Figure 10. When the resistors Rm are in place, the TECCRT pin is used for controlling the TEC

Pin #	Pin Name	Type	Description
			voltage directly. This pin can be utilized for monitoring the voltage across the TEC: TEC voltage = $V_{TECmax} \times (1 - 2 \times V_{TECCRT}/V_{VPS})$. The output impedance of this pin is 5kΩ.
6	**VTEC**	Analog output	TEC voltage indication. When the Rm's mentioned above or the TECCRT is not used for controlling the output TEC voltage directly, this pin can be utilized for monitoring the output voltage across the TEC: TEC voltage = $V_{TECmax} \times (1 - 2 \times V_{TEC}/V_{VPS})$. The maximum driving current of this pin is 30mA and the output voltage swing is 0V to V_{VPS}.
7	**CMIN**	Analog input	Compensation input pin for the thermal control loop. Connect the compensation network to this pin as shown in Figure 10 or leave it unconnected if the TEC controller has an internal compensation network already. This pin is noise sensitive. Do not connect this pin with a long wire in the air or long trace on the PCB when laying out the board for the TEC controller.
8	**TEMP**	Analog output	Actual target object temperature indication. It swings from 0V to V_{VPS}. By a default internal temperature network, it represents 15°C to 35°C when this pin's voltage swings 0V to 3V linearly; when changing from 0V to 5V, it represents 15°C to 50°C in temperature, see Figure 20 and Figure 21.
9	**SDNG**	Digital input	Shut down control. When being pulled to <0.8V, it shuts down the controller. Leaving it unconnected or pulling it >1.8V to activate the controller. This pin is internally pulled up by a resistor of 100kΩ to VPS. Before shutting down, the controller's quiescent current is 45mA; when going down, SDNG shuts down the TECNEG output stage at 1.36V and the quiescent current becomes 26mA; At SDNG = 0.8V shuts down TECPOS output stage and the quiescent current is reduced to 6mA. When going up, SDNG = 1.0V activates the TECPOS output stage and the quiescent current comes back to 26mA; SDNG = 1.37V activates the TECNEG output stage and the quiescent current comes back to the full normal value of 45mA. The maximum input voltage range allowed on this pin is from 0V to 6V. **Please note** that for all the controllers manufactured **before Dec. 2010**, when $V_{SDNG} = 0$, TEMP port remains working. For the controllers manufactured **from Dec. 2010 through 2014**, when $V_{SDNG} = 0$, all the pins including TEMP will not work. For the controllers manufactured **in 2015 and later**, when $V_{SDNG} = 0$, TEMP port remains working.
10	**GND**	ground	Signal ground, it is internally connected the control ground of the whole controller and can also be used for connecting the return path of the thermistor.
11	**RTH**	Analog input	Thermistor input port, to sense target object temperature. By using the default temperature network that comes with the standard TEC controller, the thermistor is expected to have a 10kΩ @ 25°C and the R-T curve data are given in Figure 16 or similar. It's recommended to use our NTC thermistor, ATH10K1R25.
12	**TECPOS**	Analog power output	TEC positive pin. This is the power output port for connecting to TEC's positive terminal.
13	**TECNEG**	Analog power output	TEC negative pin. This is the power output port for connecting to TEC's negative terminal.
14	**PGND**	Power ground	Power ground. It is for connecting to the return rail of the power supply.
15	**PGND**	Power ground	Power ground. The same as above, it is also for connecting to the return rail of the power supply and internally connected with pin 14 above.
16	**VPS**	Power input	Positive power supply rail. Two possible values: 3.3V and 5V, depending on the module.

Table 2. Characteristic ($T_{Ambient}$=25°C and V_{VPS}=5V)

Parameter	Test Condition	Value	Unit/Note
Target object* temp. stability vs. ambient temperature	V_{maxTEC} = 5V, R_{Load} = 2Ω	0.0002	°C/°C
Offset Object temperature vs. set-point temperature	$T_{Ambient}$ is 0~50°C Set-point temp. is 15°C ~35°C	±0.1°C or ±5mV	
Object temperature response time	≤0.1 to the set-point temperature at a 1°C step	<5	s
Efficiency	V_{VPS} = 5V, R_{Load} = 2Ω	≥90%	-
Max. output current	V_{VPS} = 5V, R_{Load} = 2Ω	2.5	A
Max. output voltage	V_{VPS} = 5V, R_{Load} = 2Ω	0 ~ V_{VPS}	V
PWM frequency		500	kHz
Power supply voltage	—	3.2 ~ 3.5 or 4.5 ~ 5.5 (Typically 3.3 or 5)	V
Set-point temp.** control voltage	V_{VPS} = 5V, R_{Load} = 2Ω	0.1 ~ V_{VPS}	V
Default set-point temp. range***	V_{VPS}=3V	15 ~ 35	°C
Operating temp. range	V_{VPS} = 5V, R_{Load} = 2Ω	−40 ~ 85	°C

* Target object temperature refers to the actual temperature of the object mounted on the cold side the TEC and its temperature is regulated by the TEC controller. This target object is often made of a metal plate on which a laser diode or an optical component is mounted.

** Set-point temperature is the desired temperature for the target object.

*** Can be customized to almost any range according to users' special needed, provided the TEC has enough thermal power to achieve the range.

**** This TEC controller can only drive the TECs with > 1Ω impedance, which can be calculated by V_{MAX}/I_{MAX}.

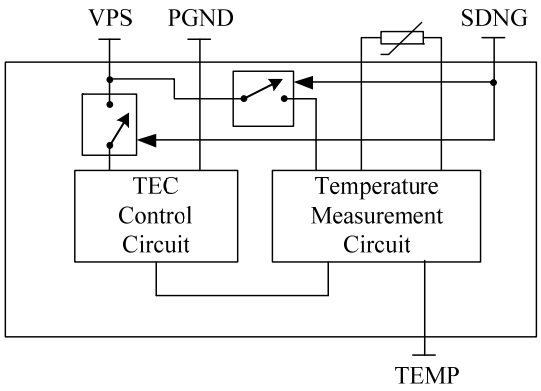


Figure 8. TEMP Does Not Work @ SDNG = 0

For all TECA1-XV-XV-D, which TEMP does not work @ SDNG = 0

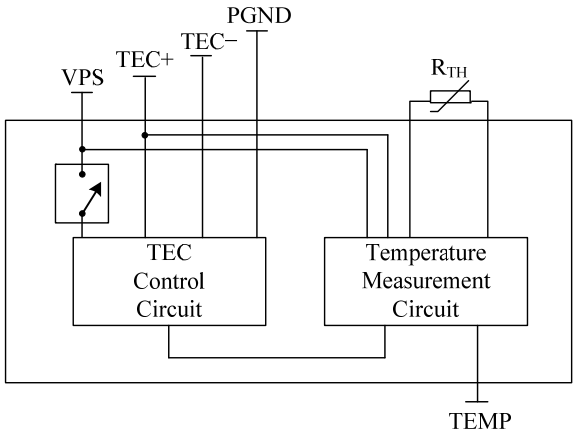


Figure 9. TEMP Work @ SDNG = 0

Only for TECA1-XV-XV-DA, which TEMP work @ SDNG = 0

APPLICATIONS

TEC controller connections are shown in Figure 10.

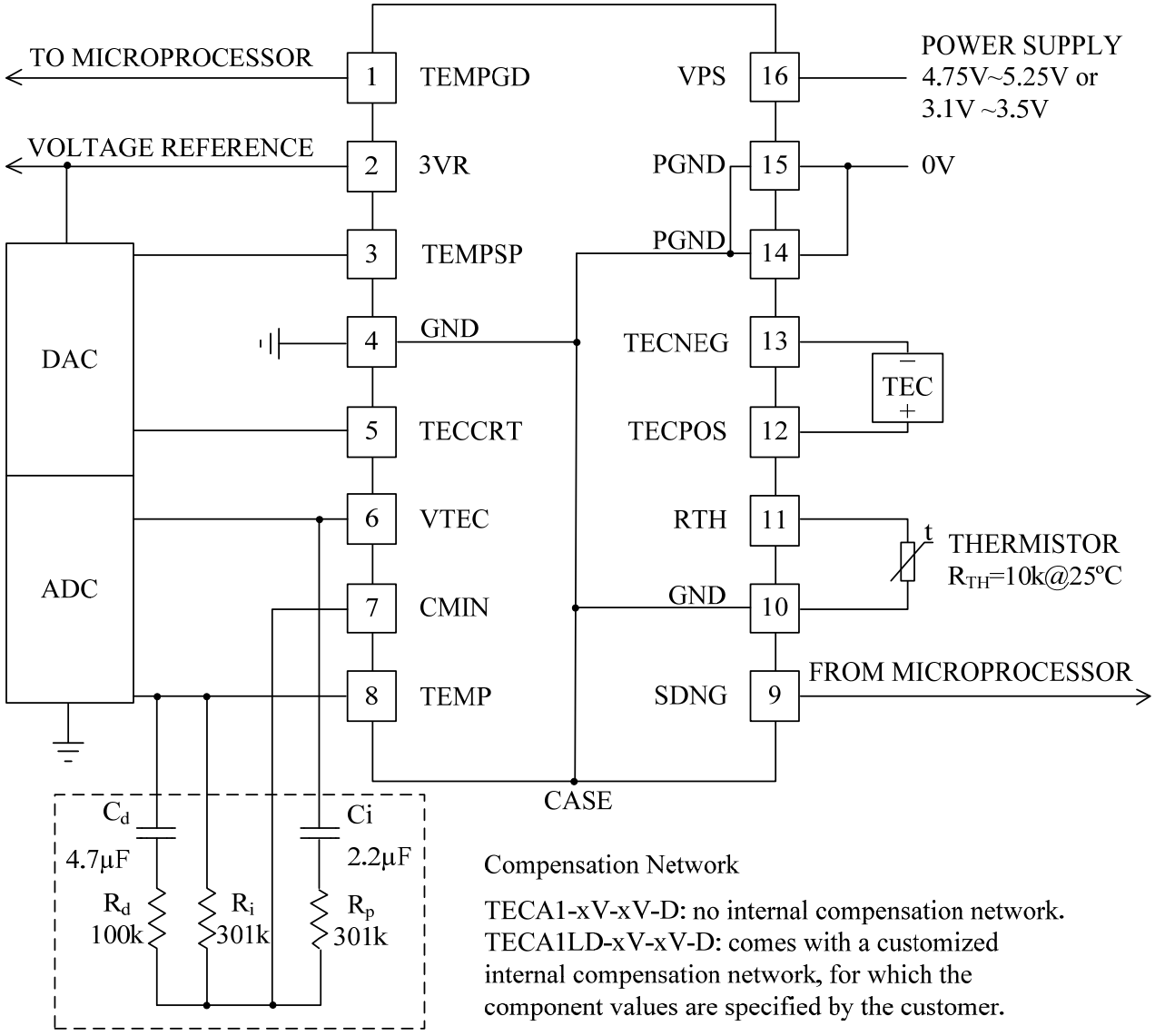


Figure 10.Microprocessor Based Application Circuit

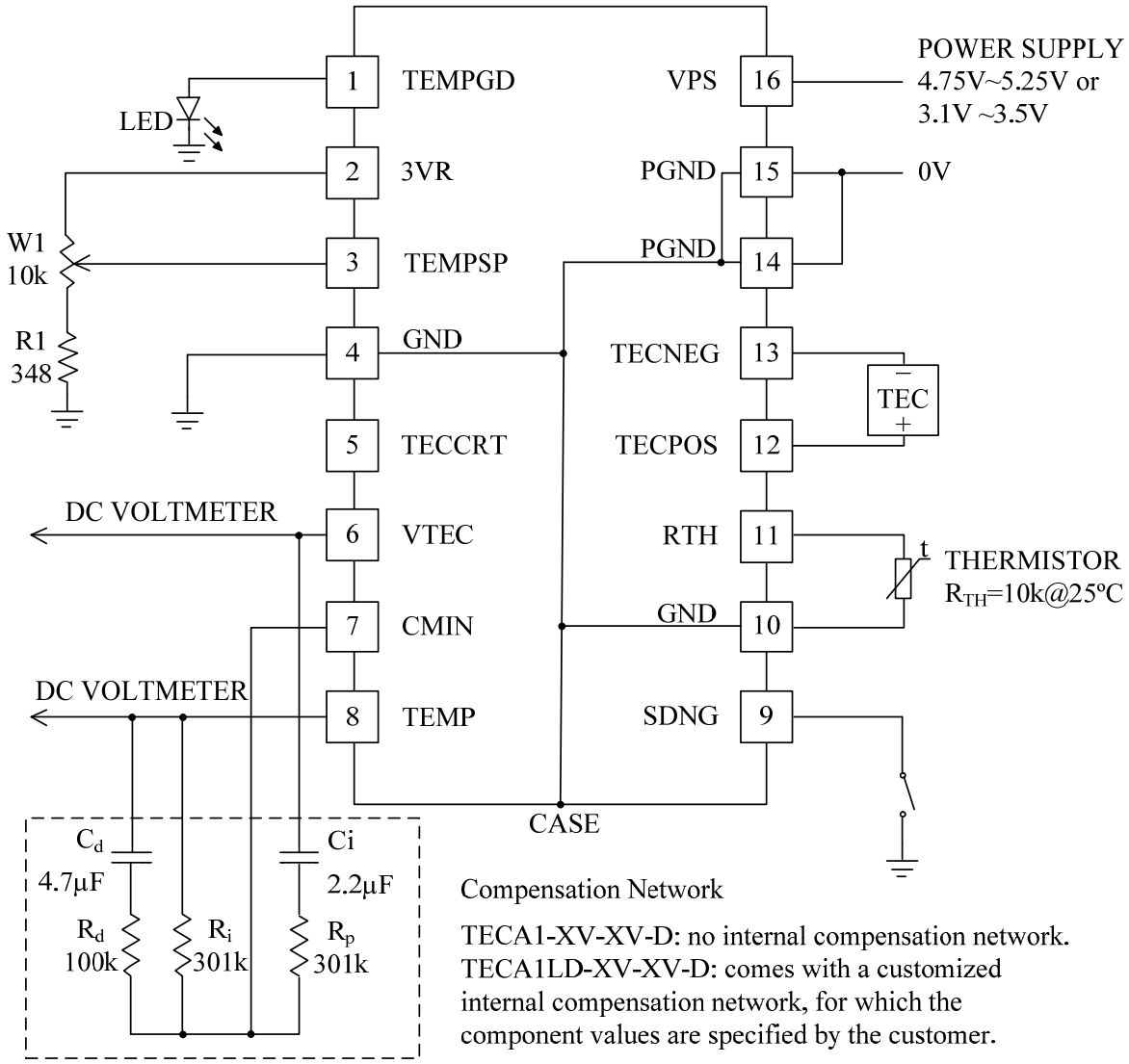


Figure 11.Stand-Alone Application Circuit

When the TEC controller is used stand-alone, a POT or a pair of resistors can be used for setting the set-point temperature by setting voltage on pin TEMPSP as shown in Figure 11. The input voltage range on the TEMPSP pin must be >0.1V and the maximum voltage on this pin is V_{VPS} – 0.2V. It is recommended to set the voltage by using the built-in 3V voltage reference, the maximum voltage is then limited to 3V. The VTEC can be utilized for measuring the voltage across the TEC as described in Table 2. The actual object temperature can be monitored by measuring the voltage on the TEMP pin. The relationship between the actual target object temperature and the TEMP voltage is determined by the internal temperature network. When using the default temperature network, the relationship is shown in Figure 11, the approximate formula is:

$ß = \log_{10}(R_oT_1/R_oT_2) / [(1/T_1 – 1/T_2) \times \log_{10}e]$

R_oT_1 stands for the zero power resistance at absolute temperature T_1

R_oT_2 stands for the zero power resistance at absolute temperature T_2

T_1 is the temperature 1, expressed in degree Kelvin.

T_2 is the temperature 2, expressed in degree Kelvin.

Despite of the non-linearity of the thermistor resistance vs. its temperature, the actual output voltage and approximated voltage is 0.013V at the worst error point, equivalent to 1.3% error.

If this TEC controller is to be used for other applications not discussed here, such as use it with wave locker controllers, please consult with us and we can help.

The TECA1-XV-XV-D controller comes with a default temperature setting network, it sets the set-point temperature to be between 15°C to 35°C when setting the TEMPSP pin voltage to be between 0V to 3V linearly and using a specific de-facto "standard" 10k @ 25°C thermistor, with its R-T value data listed in Figure 16 and Table 3. When using different thermistors and/or needing different set-point temperature ranges, please contact us, we will configure the internal temperature network for you.

In order to change the set-point temperature, an external resistor can be used to combine with your thermistor to make it equal to 10kΩ. For example, at 4°C, the thermistor is about 25kΩ, add another resistor in parallel, therefore, the total resistance is 10kΩ. After this, set the set-point temperature pin, TEMPSP, to 1.5V, the actual set-point temperature will be about 4°C. At 37°C, the thermistor is about 5kΩ, put an external resistor 5kΩ in series with this thermistor, therefore, the total resistance will be about 10kΩ at 37°C. Now, set TEMPSP pin to 1.5V, the actual set-point temperature will be about 37°C.

When using, users need to connect the pins of VTEC and CMIN together. Connect the TEMPSP pin to DAC. About ADC, users can figure it yourself.

Note: A socket strip can be used for mounting this TEC controller. More detail technical data about this socket can be found here:
http://www.digikey.com/product-detail/en/SS-132-G-2/SAM1115-32-ND/1105559

Using TEC Controllers for Driving A Heater

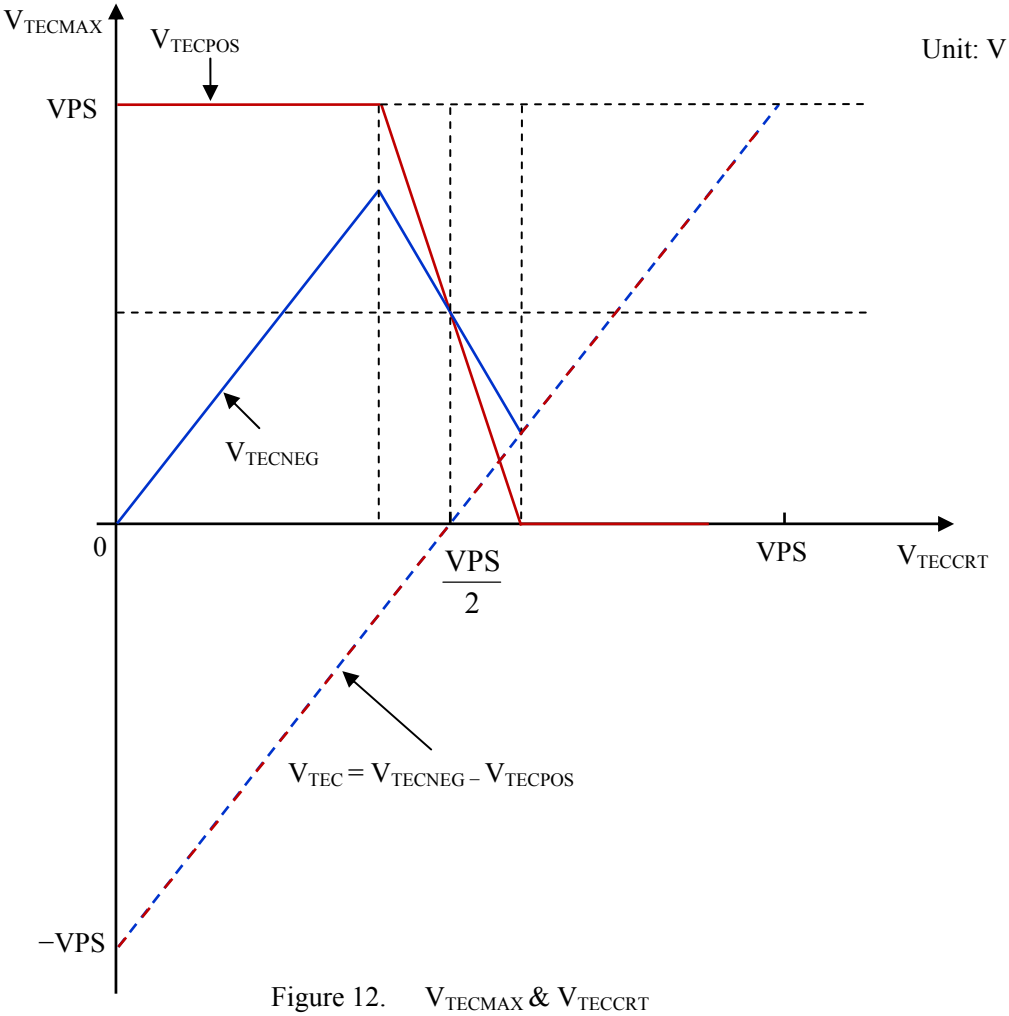
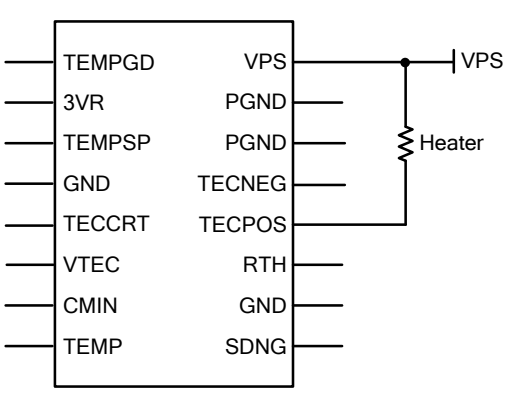


Figure 12. V_{TECMAX} & V_{TECCRT}



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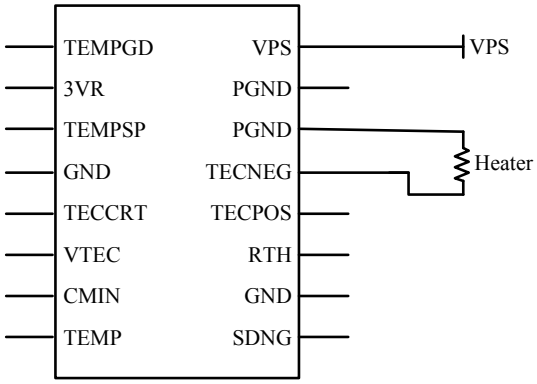

(Date: after 2/17/2022)

Figure 13. Driving a Heater between 3.3V to 5.5V

If V_{HTMAX} is 3.3V, 5V, or between 3.3V~5.5V, use TECA1-5V-5V-D. $V_{VPS}=V_{HTMAX}$; $5.5V \geq V_{VPS} \geq 3.3V$; $I_{HTMAX} \leq 3A$.

Where V_{HTMAX} stands for the maximum voltage of the heater; I_{HTMAX} stands for the maximum current of the heater.

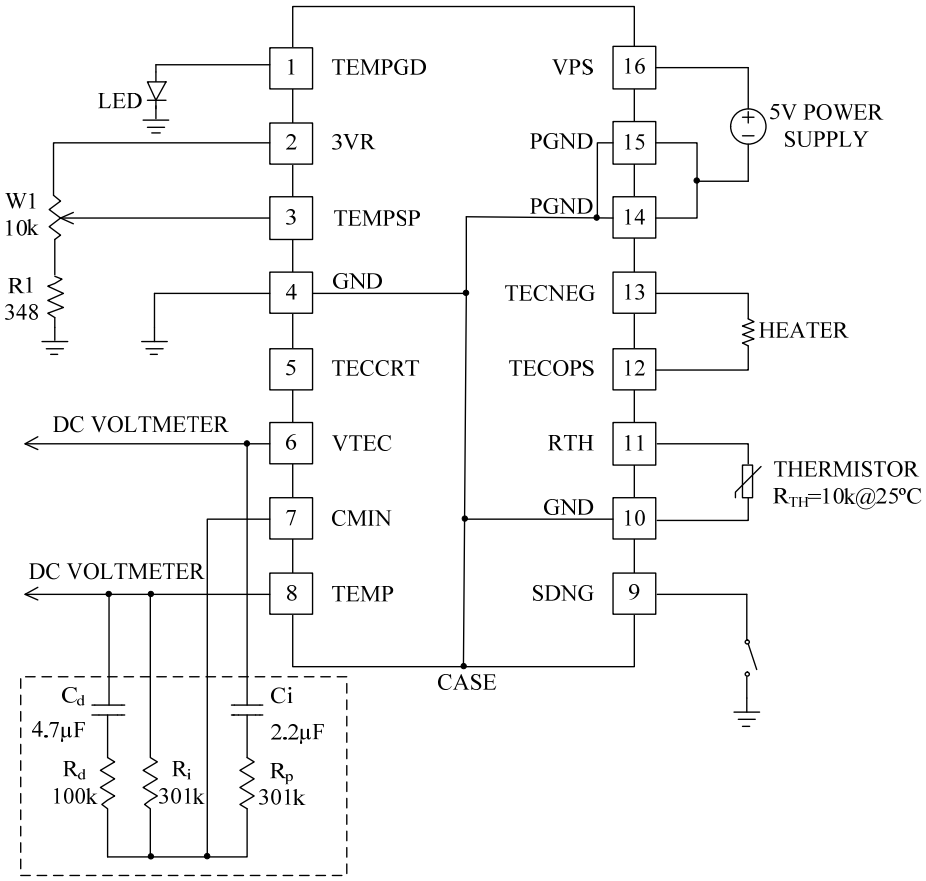

Figure 14. Driving a Heater for <3.3V @ ≤3A

If V_{HTMAX}<3.3V, the part # is TECA1-5V-[V_{HTMAX}]V-D. For example, V_{HTMAX}=2.5V, the part number will become: TECA1-5V-2.5V-D, when using a 5V power supply. If powered by a 3.3V power supply, the part number will be: TECA1-3V-2.5V-D.

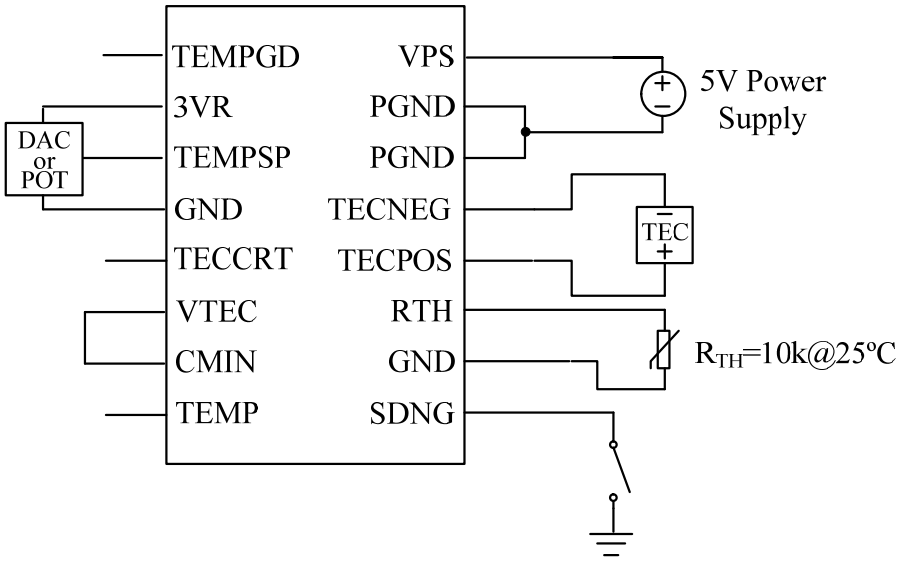

Figure 15. Control the Current Direction of the TEC Module by Pin 3 TEMPSP

When $V_{TECPOS}-V_{TECNEG} > 0$, it is forward current, which cools the object down;
When $V_{TECPOS}-V_{TECNEG} < 0$, it is reverse current, which heats the object up;
The relationship between V_{TEMPSP} and $(V_{TECPOS}-V_{TECNEG})$ is: $(V_{TECPOS}-V_{TECNEG}) = (-V_{HTMAX}/V_{VPS})\times 2\times V_{TEMPSP}+V_{HTMAX}$
For example, TECA1-5V-3V-DAH, when $V_{TEMPSP}=2V$, $(V_{TECPOS}-V_{TECNEG}) = (-3/5)\times 2\times 2+3 = 0.6V$. Note: $V_{TEMPSP}=0V\sim V_{VPS}$

TYPICAL CHARACTERISTICS

Table 3. Measurement Data of Rth vs. Temperature

Temperature (°C)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Rth (kΩ)	32.74	31.1	29.57	28.11	26.73	25.43	24.21	23.04	21.94	20.91	19.92	18.98	18.1	17.26	16.47	15.72	15
Temperature (°C)	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
Rth (kΩ)	14.33	13.68	13.07	12.49	11.94	11.42	10.92	10.45	10	9.57	9.17	8.78	8.41	8.06	7.72	7.40	7.10
Temperature (°C)	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
Rth (kΩ)	6.81	6.53	6.27	6.02	5.78	5.55	5.33	5.12	4.92	4.73	4.55	4.37	4.21	4.05	3.89	3.75	3.61

Table 4. Measurement Data of Rth vs. V_{TEMP}.

V_{TEMP} (V)	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2	1.3	1.4	1.5
Rth (kΩ)	15.72	14.80	14.33	13.91	13.49	13.07	12.70	12.32	11.94	11.60	11.26	10.92	10.62	10.31	10.00
V_{TEMP} (V)	1.6	1.7	1.8	1.9	2.0	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	2.9	3.0
Rth (kΩ)	9.73	9.45	9.17	8.91	8.66	8.41	8.18	7.95	7.72	7.52	7.31	7.10	6.91	6.72	6.53

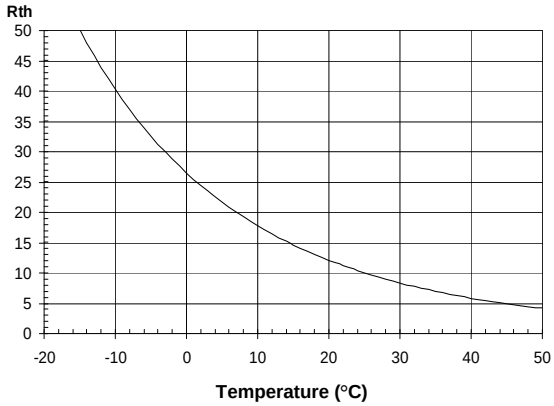

Figure 16. Rth vs. Temperature

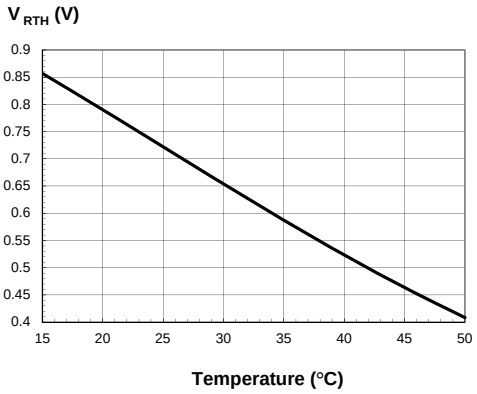

Figure 17. V_{Rth} vs. Temperature

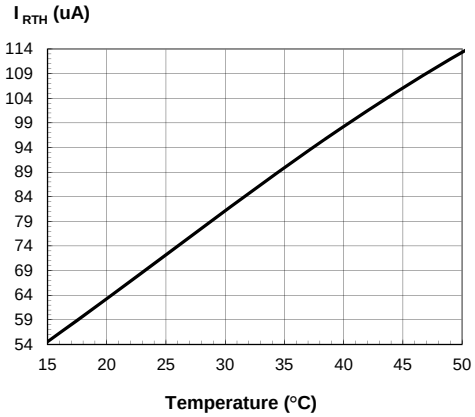

Figure 18. I_{Rth} vs. Temperature

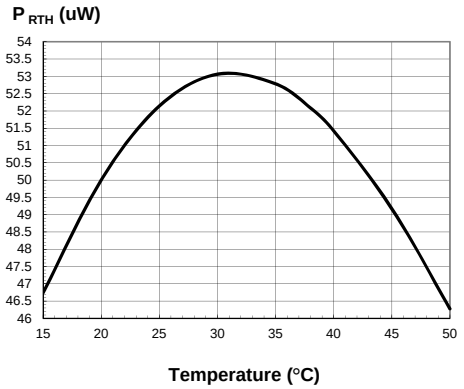

Figure 19. P_{Rth} vs. Temperature

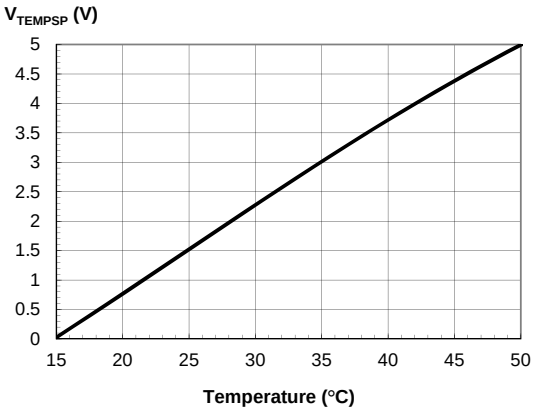

Figure 20. V_{TEMPSP} (0V−5V) vs. Temperature

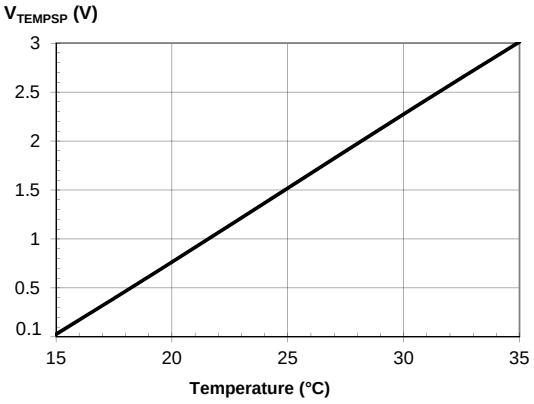

Figure 21. V_{TEMPSP} (0.1V−3V) vs. Temperature

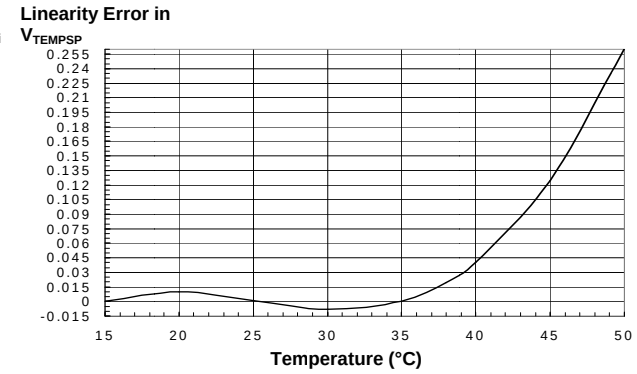

Figure 22. Linearity Error in V_{TEMPSP} vs. Temperature

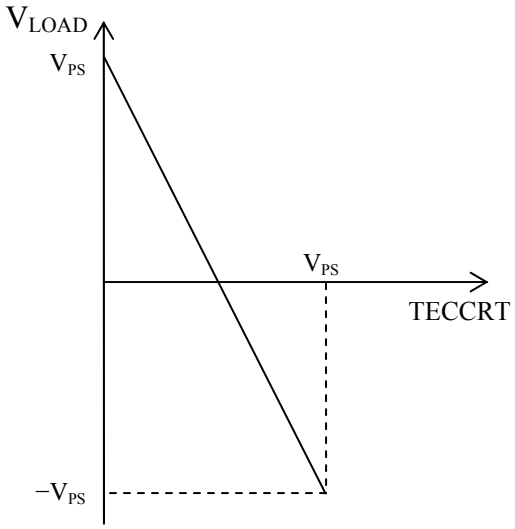

Figure 23. V_{Load} vs. TECCRT

Figure 23 shows the relationship between V_{Load} and TECCRT. With the increase of the voltage of TECCRT pin, V_{Load} will decrease linearly. The approximate formula is V_{Load} = TECPOS – TECNEG. When the TECCRT voltage reaches half of V_{VPS}, V_{Load} is zero; when it reaches VPS, the voltage will be $-V_{VPS}$.

In order to conveniently show the customers the characteristics of TECA1-XV-XV-D, we offer the efficiency curves. Figure 24 shows the relation between Output Voltage and Efficiency, Figure 25 shows the relation between Output Current and Efficiency. V_{OUT}=4V.

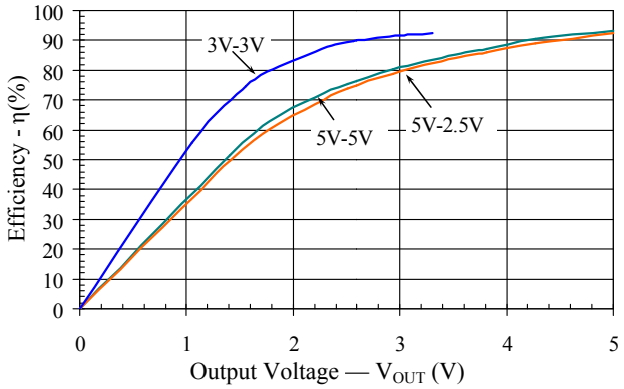

Figure 24. Efficiency vs. V_{OUT}

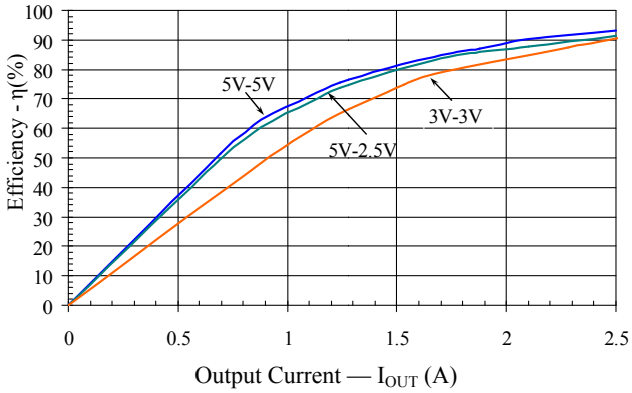

Figure 25. Efficiency vs. I_{OUT}

MECHANICAL DIMENSIONS

The controller comes in two packages: one is DIP (Dual Inline Package) or D (short for DIP) package, and the other is SMT (Surface Mount Technology) or S (short for SMT) package. The former D package comes with a part number: TECA1-XV-XV-D, and the latter S package comes with a part number: TECA1-XV-XV-S. Dimensions of the DIP package and SMT package controller are shown in Figure 26 and Figure 27 respectively.

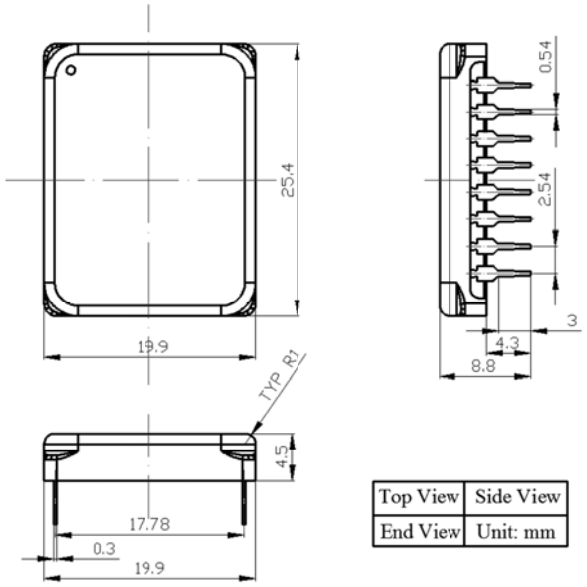

Figure 26. Dimensions of the DIP Package Controller of TECA1-XV-XV-D

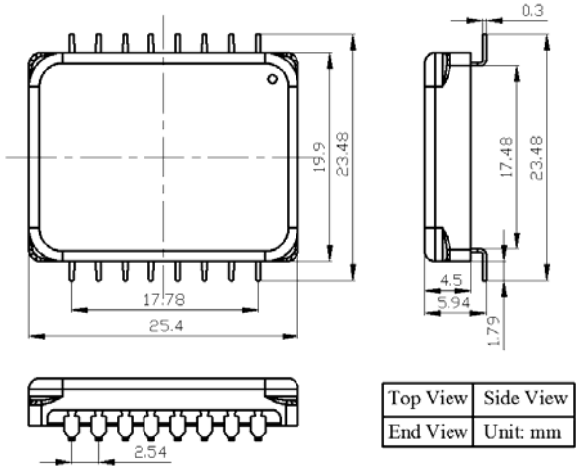

Figure 27.Dimensions of the SMT Package Controller of TECA1-XV-XV-S

CUSTOMIZATIONS

It is often found that some of the default specifications do not meet our users' particular need. We offer customizations on these specifications:

1. Maximum output voltage across TEC. When ordering, the part number will become: TECA1-5V-(max. TEC voltage)-D. E.g., TECA1-5V-2.5V-D
2. Set-point temperature range. When ordering, specify the lower limit, the upper limit, and the open circuit temperature. The part number will become: TECA1-5V-2.5V- (lower temp. limit)/(upper temp. limit)/(open circuit temp.), where lower temp. limit is the temperature corresponding to **TEMPSP** = 0V; upper temp. limit is the corresponding to **TEMPSP** = 3V; open circuit temp. corresponding to **TEMPSP** = 1.5V or being left unconnected. e.g., TECA1-5V-2.5V-D (20/80/50).
3. Asymmetrical maximum TEC voltage. The maximum TEC voltage for heating and cooling are not the same. When ordering, the part number will become: TECA1-5V- (max. TEC voltage for cooling/Max. TEC voltage for heating), e.g. TECA1-5V-2.5V/1.5V-D.

WARNING: This controller module can only be soldered manually on the board by a solder iron at < 310°C (590°F), and it cannot go through a reflow oven process.

NOTE: The power supply may have overshoot, when happens, it may exceed the maximum allowed input voltage, 6V, of the controller and damage the controller permanently. To avoid this from happening, do the following:

1. **Connect the controller solid well with the power supply before turning on the power.**
2. **Make sure that the power supply has sufficient output current. It is suggested that the power supply can supply 1.2 to 1.5 times the maximum current the controller requires.**
3. **When using a bench top power supply, set the current limit to >1.5 times higher than the maximum current the controller requires.**

If a higher precision TEC controller is needed, TECA1-XV-XV-DAH meets your need. please check the info. below.

Part #	Maximum $\lvert V_{TEMP} - V_{TEMPSP} \rvert$ (mV)
TECA1-XV-XV-DAH	≤0.5
TECA1-XV-XV-D	≤5

ORDERING INFORMATION

Table 5. Ordering info.

Part Number	Internal Compensation Network	Description	Difference
TECA1-5V-XV*-D/S	No	5V power supply in DIP/SMT package	TEMP pin remains on @SDNG=0 Maximum output voltage across TEC can be selected from 5V, 4.8V, 4V, 3.5V, 3V, 2.5V and 2V or required one.
TECA1LD-5V-XV*-D/S	Yes		
TECA1-3V-XV*-D/S	No	3.3V power supply in DIP/SMT package	TEMP pin remains on @SDNG=0 Maximum output voltage across TEC can be selected from 3V, 2.5V and 2V or required one.
TECA1LD-3V-XV*-D/S	Yes		
TECA1-XV-XV-D-OP	No	Remove two 10MΩ internal resistors; DIP package	TEMP pin remains on @SDNG=0 Maximum output voltage across TEC can be selected from 5V, 4.8V, 4V, 3.5V, 3V, 2.5V and 2V or required one.
TECA1-5V-XV*-DAH	No	5V power supply in DIP package	**High precision** TEMP pin remains on @SDNG=0 Voltage difference between TEMP and TEMPSP is −0.02mV ~ 0.5mV, ten times lower than TECA1-5V-xV-D, 4~5mV.
TECA1LD-5V-XV*-DAH	Yes		
TECA1-3V-XV*-DAH	No	3.3V power supply in DIP package	
TECA1LD-3V-XV*-DAH	Yes		
TECA1-XV-XV*-DAH-OP	No	Remove two 10MΩ internal resistors; DIP package	**High precision** TEMP pin remains on @SDNG=0 Maximum output voltage across TEC can be selected from 5V, 4.8V, 4V, 3.5V, 3V, 2.5V and 2V or required one.

*XV stands for the maximum output voltage across TEC. e.g. TECA1-5V-3.5V-D.

SPECIAL NOTE

If you experience a high current spike when you change TEMPSP voltage quickly by a large amount, such as > 0.1V, a capacitor of 1uF can be added between TECCRT and GND. For TEC controllers manufactured after Nov. 10, 2015, there is no such a problem.

EVALUATION BOARD

Part #	Description	Comments
TECEV104	Evaluation Board TECEV104 for TEC Controllers TECA1-XV-XV-D	1. Setting maximum output voltage 2. Setting set-point temperature 3. Monitoring output voltage 4. Monitoring actual thermal load temperature 5. Tuning the compensation network so as to match thermal load

RELATED PRODCUT SELECTION GUIDE

Part #	V_{IN}	V_{OUT}	Dimensions (mm)	Difference
TEC14M5V3R5AS	2.7V ~ 5.5V	$\pm V_{VPS}$	14.0×14.0×2.2	Micro TEC controller
TEC18V15A	6.0V~18V	±15V	35.7×35.7×7.2	High voltage high current with embedded firmware inside
TEC50V20ACH Under Development	12V ~ 50V	±40V	63.0×61.0×16.7	High voltage high current
TEC5V6A-D	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM; Two 100kΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 5mV$
TEC5V6A-DA	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 100kΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 2mV$
TEC5V6A-DAH	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 100kΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 0.5mV$
TEC5V6A-NT	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 100kΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network
TEC5V4A-D	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 100kΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 5mV$
TEC5V4A-DA	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 100kΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 2mV$
TEC5V4A-DAH	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 100kΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$
TEC5V4A-NT	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 100kΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network
TECA1-XV-XV-DAH	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 100kΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$
TECA1-XV-XV-DAH-OP	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 100kΩ resistors on TEMPSP pin: removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$

Part #	V_{IN}	V_{OUT}	Dimensions (mm)	Difference
TECA1LD-XV-XV-DAH	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 100kΩ resistors on TEMPSP pin: Not removed With internal compensation network Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \le 0.5mV$
TECA1-XV-XV-D	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 100kΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP - VTEMPSP}\rvert \le 5mV$
TECA1-XV-XV-D-OP	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 100kΩ resistors on TEMPSP pin: removed Max. $\lvert V_{TEMP - VTEMPSP}\rvert \le 5mV$
TECA1LD-XV-XV-D	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 100kΩ resistors on TEMPSP pin: Not removed With internal compensation network Max. $\lvert V_{TEMP - VTEMPSP}\rvert \le 5mV$
TECA1-5V5V-NT	5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 100kΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network
TECA2-XV-XV-DAH	4.5V ~ 5.5V	$\pm V_{VPS}$	20.14×14.6×8.0	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 100kΩ resistors on TEMPSP pin: Not removed Smaller size

NOTICE

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