High Efficiency 2.5A TEC Controller

TECA1-5V5V-NT

Figure 1. The Photos of Actual TECA1-5V5V-NT

FEATURES

- High Efficiency: ≥90%
- Maximum Output Current: 2.5A
- Actual Object Temperature Monitoring
- High Stability: 0.01 ℃
- High Reliability and Zero EMI
- Compact Size
- 100% lead (Pb)-free and RoHS compliant

DESCRIPTION

The TECA1-5V5V-NT is an electronic module designed for driving TECs (Thermo-Electric Coolers) with high stability in regulating an object's temperature, high energy efficiency, zero EMIs, and small package. It can be used in a vacuum environment. Figure 1 is the photo of an actual TECA1-5V5V-NT TEC controller.

This module provides interface ports for users to set the desired object's temperature, i.e. set-point temperature; the maximum output voltage across TEC; and the compensation network. The compensation network makes automatic adjustments for any deficiencies to achieve and maintain high order thermal load and thus stabilizes temperature control loop.

It provides these functions: thermistor T-R curve linearization, temperature measurement and monitoring, temperature control loop status indication, TEC voltage monitoring, power up delay, and shut down.

The TECA1-5V5V-NT comes with a high stability low noise 3.0V voltage reference, which can be used for setting the desired object's temperature by using a POT (Potentiometer) or a DAC (Digital to Analog Converter). When using this reference for setting the set-point temperature, the set-point temperature error is independent of this reference voltage. This is because internal temperature measurement network also uses this voltage as the reference, the errors in setting the temperature and measuring the temperature cancel with each other, setting the object's temperature with higher stability. This reference can also be utilized by an ADC (Analog to Digital Converter), for the same reason, the measurement error will also be independent of the reference voltage, resulting in a more accurate measurement. Figure 2 is the real size top view of the controller showing the pin names and locations. The functions of all the pins are shown in Table 1.

Warning: This controller module can only be soldered manually onto the board by a solder iron at < 310 ℃ (590°F), it cannot go through a reflow oven process.

The TECA1-5V5V-NT is packaged in a 6-sided metal enclosure, which blocks EMIs (Electro-Magnetic Interferences) to prevent the controller and other electronics from interfering with each other.

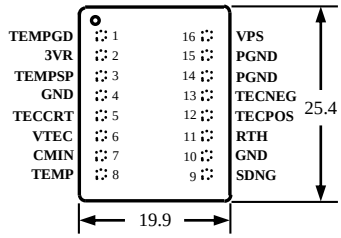

Figure 2. Pin names and Locations

SPECIFICATIONS

Table 1. Pin Function Descriptions

Pin #	Pin Name	Type	Description
1	**TEMPGD**	Digital output	Temperature good indication. It is pulled high when the set-point temperature and the actual desired object temperature are <0.1°C in temperature difference when the set-point temperature range is 20°C; or <0.5mV in voltage difference between the voltages of TEMP and TEMPSP nodes. It is internally pulled up or down a 130Ω and a 90Ω resistor respectively when goes up and down. It can be used to drive LEDS as indications.
2	**3VR**	Analog output	Reference voltage output, 3V. It can be used by a POT or DAC for setting the set-point temperature voltage on the TEMPSP pin and/or a DAC for measuring the temperature through the TEMP pin. The maximum sourcing current capability is 1.5mA and the maximum sinking is 4mA with a stability of <50ppm/°C max.
3	**TEMPSP**	Analog input	Object set-point temperature input port. It is internally tied to a voltage divider formed by two 100kΩ resistors to reduce the reference by half, equals to 1.5V. It is highly recommended to set this pin's voltage by using the controller's voltage reference. The lower limit of the setting voltage for this pin is 0.1V. Setting this pin to a <0.1V voltage may cause the controller over cooling the object. This pin can also be set to a voltage that is about 0.2V away from the VPS rail. This pin can be set by using a POT or DAC.
4	**GND**	Ground	Signal ground for the POT, ADC, DAC and the thermistor, see Figure 4.
5	**TECCRT**	Both analog input and output	TEC control voltage. It can be left unconnected or used to control the TEC voltage directly. Set TECCRT between 0V to VPS, the voltage across TEC will be: TEC voltage = 2×TECCRT / VPS. It can also be used to configure the maximum voltage cross the TEC: Max. TEC voltage = V_{TEC_Max} × Rm / (Rm+10k), where V_{TEC_Max} is the maximum output voltage of the TEC controller configured by the internal limiting circuit when the controller is released by the factory, it is marked on the TEC controller label; Rm is the resistance of the two resistors one between TECCRT to GND and the other between TECCRT to VPS, as shown in Figure 4. When the resistors Rm are in place, the TECCRT pin is used for controlling the TEC voltage directly. This pin can be utilized for monitoring the voltage across the TEC: TEC voltage = V_{TEC_Max} × (1 – 2×TECCRT/VPS). The output impedance of this pin is 5kΩ.
6	**VTEC**	Analog output	TEC voltage indication. When the Rm's mentioned above or the TECCRT is not used for controlling the output TEC voltage directly, this pin can be utilized for monitoring the output voltage across the TEC: TEC voltage = V_{TEC_Max} × (1 – 2×V_{TEC}/VPS). The maximum driving current of this pin is 30mA and the output voltage swing is 0V to VPS.
7	**CMIN**	Analog input	Compensation input pin for the thermal control loop. Connect the compensation network to this pin as shown in Figure 4 or leave it unconnected if the TEC controller has an internal compensation network already. This pin is noise sensitive. Do not connect this pin with a long wire in the air or long trace on the PCB when layout the board for the TEC controller.
8	**TEMP**	Analog output	Actual object temperature indication. It swings from 0V to VPS.
9	**SDNG**	Digital input	Shut down control. When pulled low, it shuts down the controller. Leave it open or pull it high to activate the controller. The threshold voltage is 0.8V. This pin is internally pulled up by a resistor of 100k to VPS. The threshold voltages of this pin are: before shuts down, the quiescent current is about 45mA; when going down, SDNG = 1.36V shuts down the TECNEG output stage and the quiescent current becomes 26mA; SDNG =

			0.8V shuts down TECPOS output stage and the quiescent current becomes 6mA; when going up, SDNG = 1.0V activates the TECPOS output stage and the quiescent current goes back to 26mA; SDNG = 1.37V activates the TECNEG output stage and the quiescent current goes back to the full normal value of 45mA. The maximum input voltage range allowed on this pin is from 0V to 6V.
10	**GND**	ground	Signal ground, internally connected to Pin 4 GND. It can be used for connecting the return path of the thermistor.
11	**RTH**	Analog input	Inverting input to error amplifier.
12	**TECPOS**	Analog power output	Connects to TEC positive terminal
13	**TECNEG**	Analog power output	Connects to TEC negative terminal
14	**PGND**	Power ground	Power ground for connecting to the power supply
15	**PGND**	Power ground	Power ground for connecting to the power supply, internally connected with pin 14
16	**VPS**	Power input	Positive power supply rail. Two possible values: 3.3V and 5V, depending on the module.

Table 2. Characteristic ($T_{Ambient}$=25°C)

Parameter	Test Condition	Value	Unit/Note
Object* temp. stability vs. ambient temp	V_{VPS} = 5V, R_{Load} = 2Ω	0.0002	°C/°C
Offset Object temp. vs. set-point temp.	$T_{Ambient}$ is 0~50°C Set-point temp. is 15°C ~35°C	±0.1°C or ±5mV	
Object temp. response time	≤0.1 to the set-point temperature at a 1°C step	<5	s
Efficiency	V_{VPS} = 5V, R_{Load} = 2Ω	≥90%	-
Max. output current	V_{VPS} = 5V, R_{Load} = 2Ω	2.5	A
Max. output voltage	V_{VPS} = 5V, R_{Load} = 2Ω	0 ~ (V_{VPS} − 0.2)	V
PWM frequency		500	kHz
Power supply voltage	—	4.75 ~ 5.25 (Typically 5)	V
Set-point temp.** control voltage	V_{VPS} = 5V, R_{Load} = 2Ω	0.1 ~ V_{VPS}	V
Default set-point temp. range***	VPS=3V	15 ~ 35	°C
Operating temp. range	V_{VPS} = 5V, R_{Load} = 2Ω	−40 ~ 85	°C

* Object temperature refers to the actual temperature of the object which is mounted on the cold side the TEC and its temperature needs to be regulated by the TEC. This object is often a metal block on which a laser diode or an optical crystal is mounted.

** Set-point temperature is the temperature of the object desired to achieve.

*** Can be customized to any range according to requirement.

**** This TEC controller can only drive the TECs having > 1Ω impedance, which equals V_{MAX}/I_{MAX}.

***** After many experiments, according to the parameter and the figuring method of R_{Load}, we advise customers to use R_{Load} of 2Ω to get the ideal character. We can also make the Maximum Output Voltage reach any value of (VPS – 0.1×I_{OUT}) if you need.

BLOCK DIAGRAM

The block diagram of the controller is shown in Figure 3.

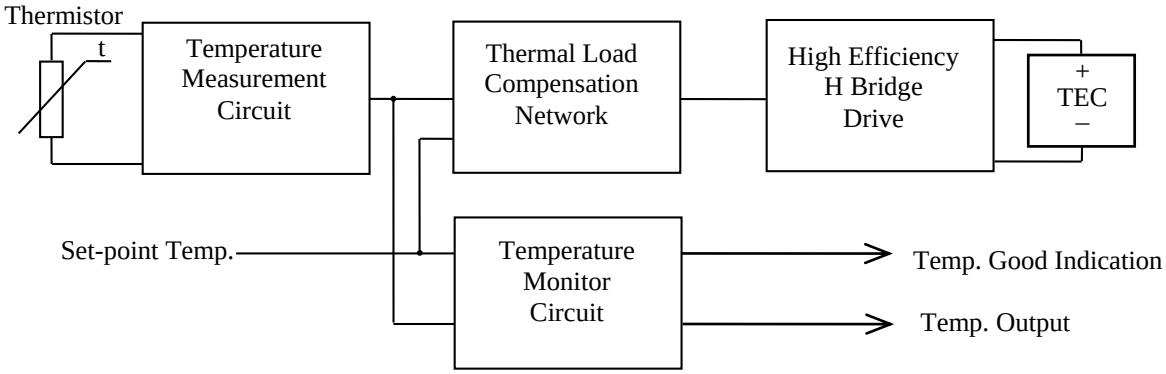

Figure 3. TEC Controller Block Diagram

APPLICATIONS

TEC controller connections are shown in Figure 4.

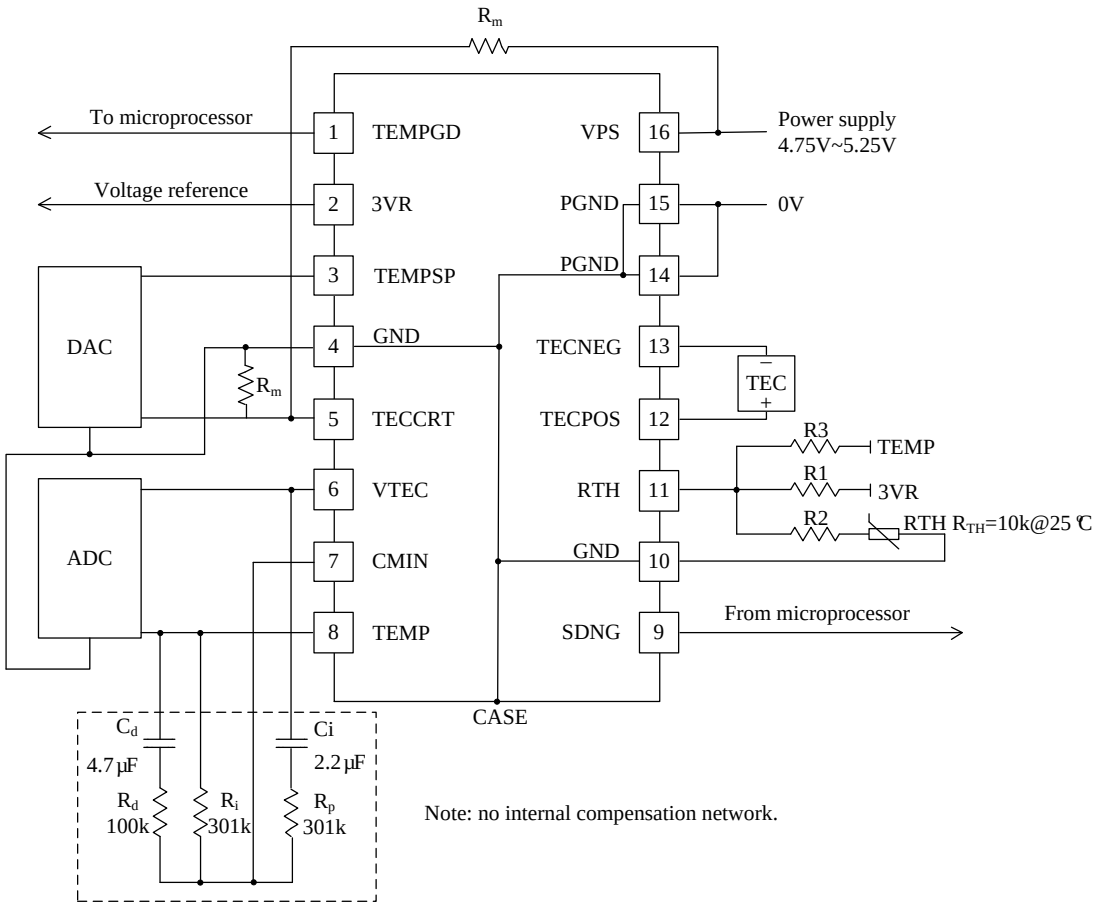

Figure 4. Microprocessor Based Application Circuit

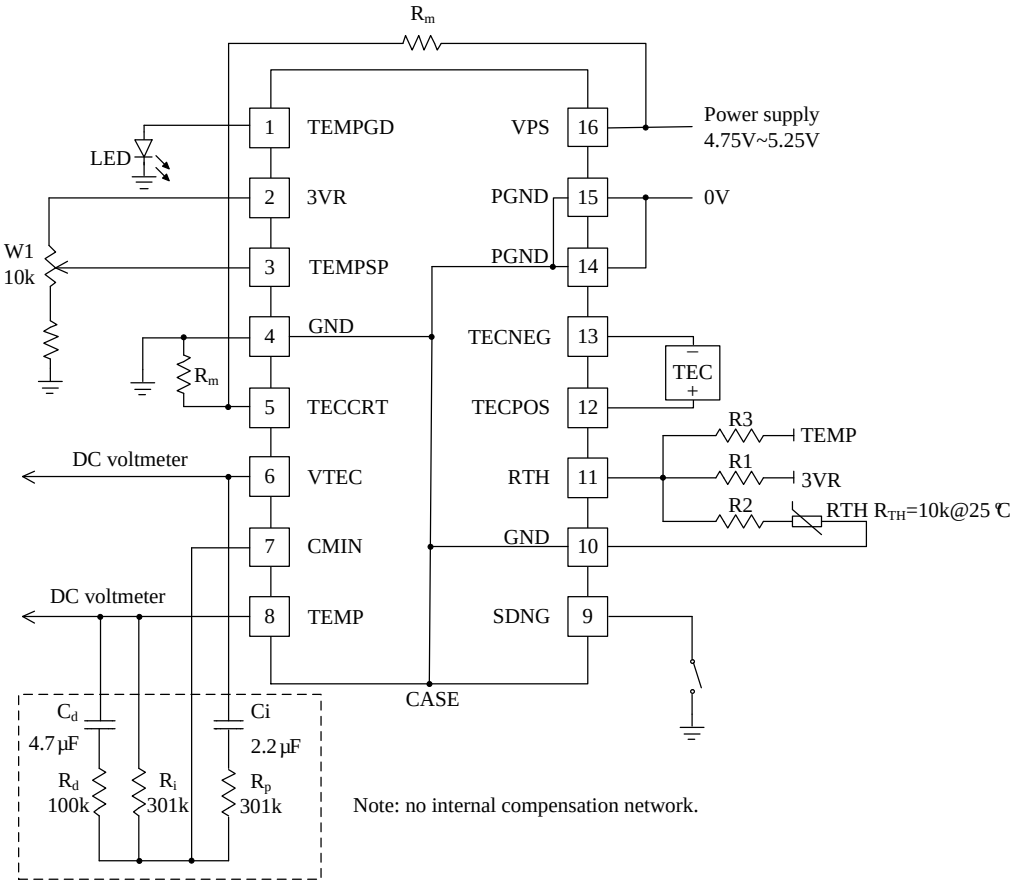

Figure 5. Stand-Alone Application Circuit

When the TEC controller is used stand-alone, using a POT or a pair of resistors to replace the POT to set the voltage for the set-point temperature pin TEMPSP as shown in Figure 5. The input voltage range on the TEMPSP pin must be >0.1V and the maximum voltage on this pin is V_{VPS} – 0.1V. The VTEC can be utilized for measuring the voltage across the TEC as described in Table 2. The actual object temperature can be monitored by measuring the voltage on the TEMP pin. The relationship between the actual temperature and the TEMP voltage is determined by the internal temperature network. When using the default temperature network, the relationship is shown in Figure 5, the approximate formula is:

$$ß = \log_{10}(R_oT_1/R_oT_2) / [(1/T_1 - 1/T_2) \times \log_{10}e]$$

R_oT_1 stands for the zero power resistance at absolute temperature T_1

R_oT_2 stands for the zero power resistance at absolute temperature T_2

T_1 is the temperature 1, expressed in degree Kelvin.

T_2 is the temperature 2, expressed in degree Kelvin.

The maximum error between the actual output voltage and approximated voltage is 0.013V, equivalent to 1.3% error.

The TEC controller doesn't come with a default temperature setting network, which allows you to specify the temperature range by using the external resistors, R1, R2 and R3.

Note: A socket strip can be used for mounting this TEC controller. More detail technical data about this socket can be found here:
http://www.digikey.com/product-detail/en/SS-132-G-2/SAM1115-32-ND/1105559

Using TEC Controllers for Driving A Heater

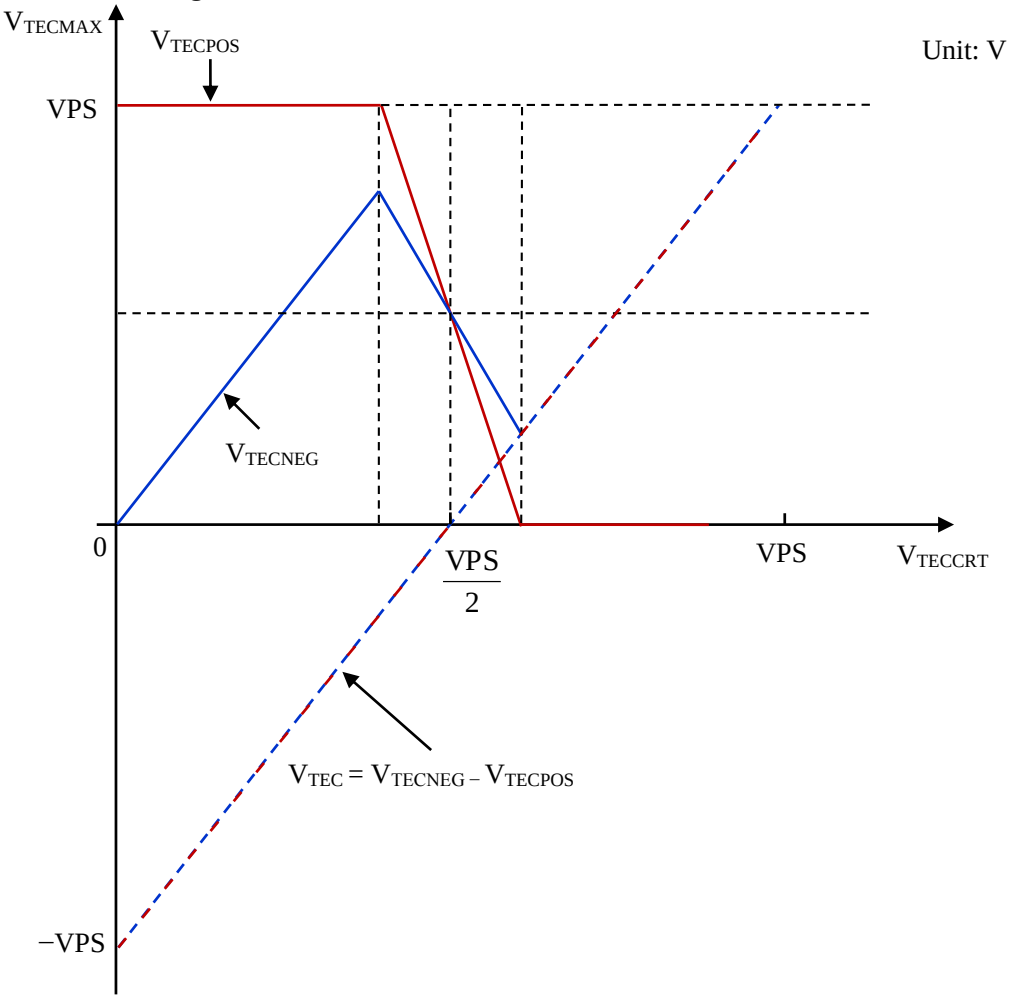

Figure 6. V_{TECMAX} & V_{TECCRT}

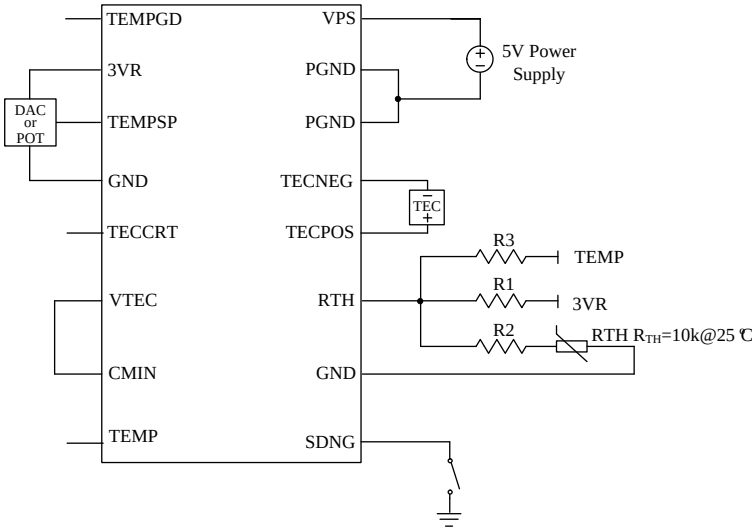

Figure 7. Control the Current Direction of the TEC Module by Pin 3 TEMPSP

When $V_{TECPOS}–V_{TECNEG} > 0$, it is forward current, which cools the object down;
When $V_{TECPOS}–V_{TECNEG} <0$, it is reverse current, which heats the object up;
The relationship between V_{TEMPSP} and $(V_{TECPOS}–V_{TECNEG})$ is: $(V_{TECPOS}–V_{TECNEG}) = (–5/5)×2×V_{TEMPSP}+5$; when V_{TEMPSP}=2V, $(V_{TECPOS}–V_{TECNEG}) = (–5/5)×2×2+5 = 1V$. Note: V_{TEMPSP}=0V~V_{VPS}.

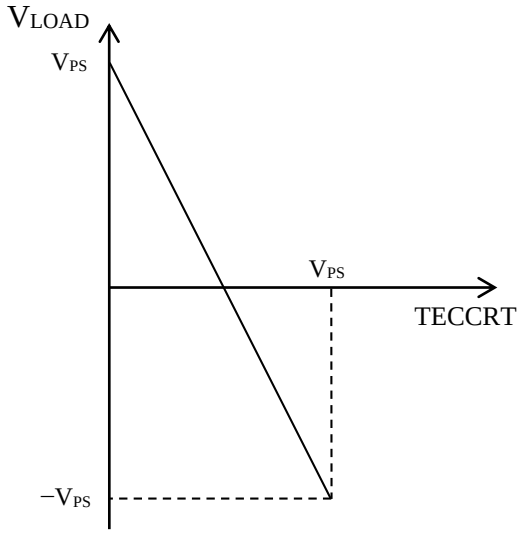

Figure 8. V_{Load} vs. TECCRT

Figure 8 shows the relationship between V_{Load} and TECCRT. With the increase of the voltage of TECCRT pin, V_{Load} will decrease linearly. The approximate formula is V_{Load} = TECPOS – TECNEG. When the TECCRT voltage reaches half of V_{PS}, V_{Load} is zero; when it reaches VPS, the voltage will be $–V_{PS}$.

In order to conveniently show the customers the characteristics of TECA1-5V5V-NT, we offer the efficiency curves. Figure 9 shows the relation between Output Voltage and Efficiency, Figure 10 shows the relation between Output Current and Efficiency. V_{OUT}=4V.

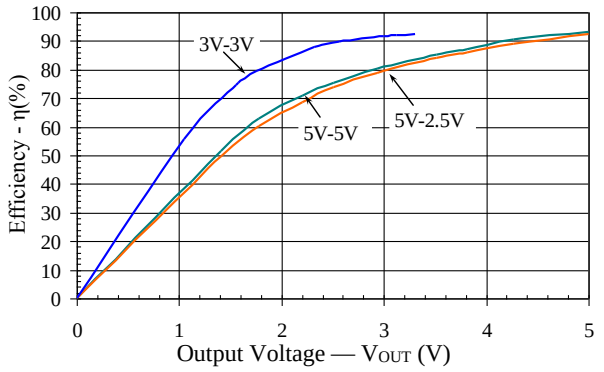

Figure 9. Efficiency vs. V_{OUT}.

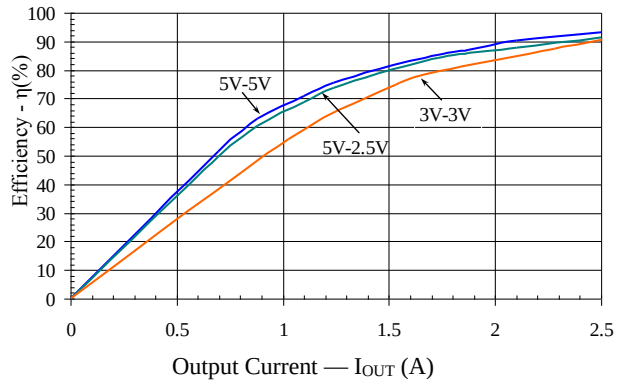

Figure 10. Efficiency vs. I_{OUT}

TEMPGD INTERNAL CIRCUIT

When temperature difference between the actual temperature and the set-point temperature < 0.1℃, the pull-up resistor R1 for TEMPGD pin is 130Ω; When temperature difference between the actual temperature and the set-point temperature > 0.1℃, the pull-down resistor R2 for TEMPGD pin is 90Ω. See Figure 11.

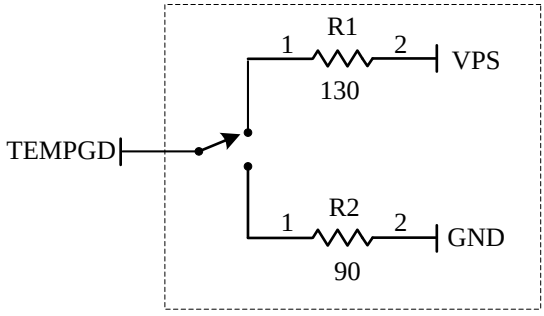

Figure 11. Internal Equivalent Circuit on TEMPGD Pin

OVERRIDE INTERNAL VOLTAGE SETTING

When the controller does not connect anything externally, the V_{TEMPSP} is 1.5V. If the controller connects a DAC or Potentiometer externally, remove the two 100kΩ resistors in the circuit in Figure 12. Please note that these two resistors are 10MΩ before June 26, 2022, and will be changed to 100kΩ after this date.

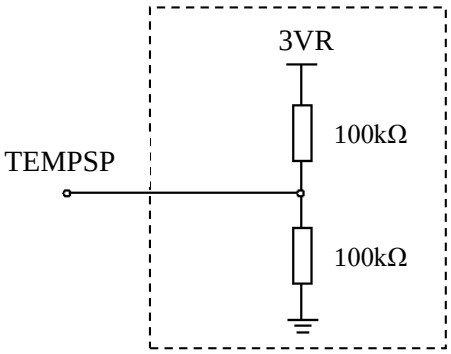

Figure 12. Internal Equivalent Circuit on TEMPSP Pin

QUIESCENT CURRENT VS. SHUTDOWN VOLTAGE

Figure 13 shows how the quiescent current (I_Q) changes with the voltage of Pin SDNG (V_{SDNG}).

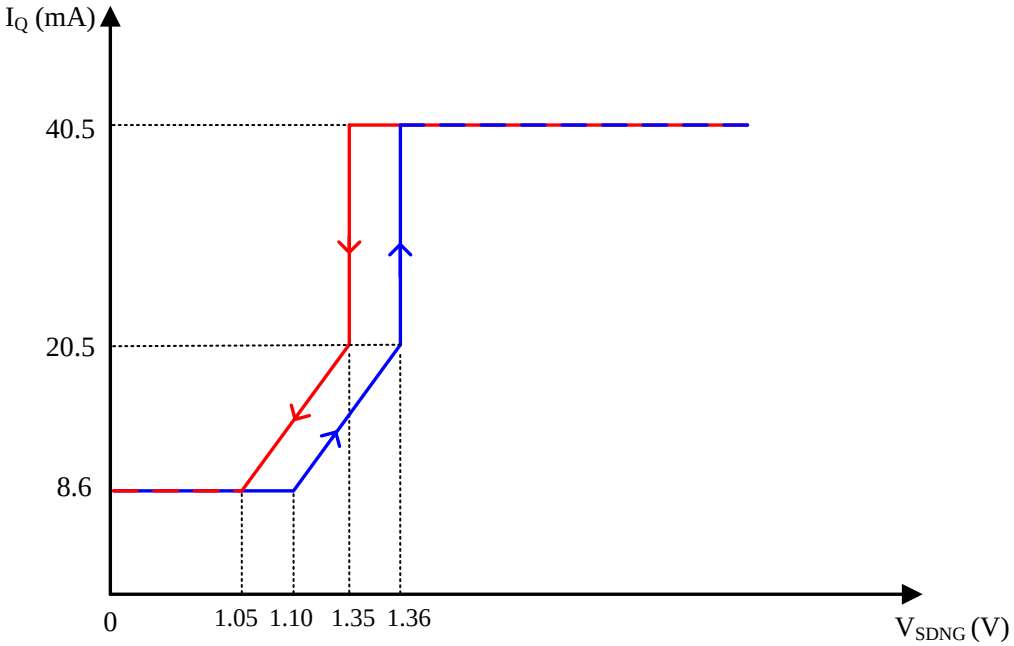

Figure 13. I_Q vs. V_{SDNG}

MECHANICAL DIMENSIONS

The controller comes in DIP (Dual Inline Package) package. Dimensions of the controller are shown in Figure 14.

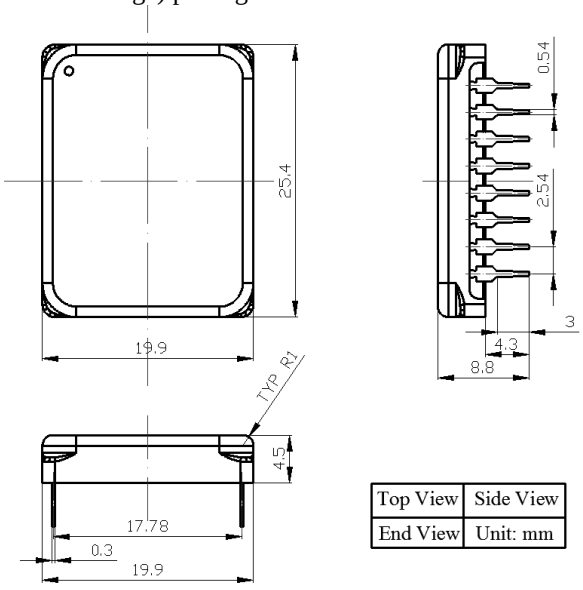

Figure 14. Dimensions of the DIP Package Controller of TECA1-5V5V-NT

WARNING: This controller module can only be soldered manually on the board by a solder iron at < 310°C (590°F), and it cannot go through a reflow oven process.

NOTE: The power supply may have overshoot, when happens, it may exceed the maximum allowed input voltage, 6V, of the controller and damage the controller permanently. To avoid this from happening, do the following:

1. **Connect the controller solid well with the power supply before turning on the power.**
2. **Make sure that the power supply has sufficient output current. It is suggested that the power supply can supply 1.2 to 1.5 times the maximum current the controller requires.**
3. **When using a bench top power supply, set the current limit to >1.5 times higher than the maximum current the controller requires.**

ORDERING INFORMATION

Table 3. Ordering info.

Part Number	Default Temperature Network	Note
TECA1-5V5V-NT	No	TEMP pin remains on @SDNG=0

RELATED PRODUCT SELECTION GUIDE

Part #	V_{IN}	V_{OUT}	Dimensions (mm)	Difference
TEC14M5V3R5AS	2.7V ~ 5.5V	$\pm V_{VPS}$	14.0×14.0×2.2	Micro TEC controller
TEC18V15A	6.0V~18V	±15V	35.7×35.7×7.2	High voltage high current with embedded firmware inside
TEC50V20ACH Under Development	12V ~ 50V	±40V	63.0×61.0×16.7	High voltage high current
TEC5V6A-D	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM; Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 5mV$
TEC5V6A-DA	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 2mV$
TEC5V6A-DAH	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leqslant 0.5mV$
TEC5V6A-NT	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network
TEC5V4A-D	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 5mV$
TEC5V4A-DA	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 2mV$
TEC5V4A-DAH	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$
TEC5V4A-NT	4.5V ~ 5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Linear; TECPOS: Filtered PWM Two 10MΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network
TECA1-xV-xV-DAH	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains on @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$
TECA1-xV-xV-DAH-OP	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: removed Max. $\lvert V_{TEMP} - V_{TEMPSP}\rvert \leq 0.5mV$

TECA1LD-xV-xV-DAH	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed With internal compensation network Max. $\lvert V_{TEMP} - V_{TEMPSP} \rvert \leq 0.5mV$
TECA1-xV-xV-D	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed Max. $\lvert V_{TEMP - VTEMPSP} \rvert \leq 5mV$
TECA1-xV-xV-D-OP	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: removed Max. $\lvert V_{TEMP - VTEMPSP} \rvert \leq 5mV$
TECA1LD-xV-xV-D	3.3V/5.5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed With internal compensation network Max. $\lvert V_{TEMP - VTEMPSP} \rvert \leq 5mV$
TECA1-5V5V-NT	5V	$\pm V_{VPS}$	25.4×19.9×8.8	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed No internal temperature range setting network
TECA2-xV-xV-DAH	4.5V ~ 5.5V	$\pm V_{VPS}$	20.14×14.6×8.0	TEMP pin remains off @SDNG=0 TECNEG: Filtered PWM; TECPOS: Linear Two 10MΩ resistors on TEMPSP pin: Not removed Smaller size

NOTICE

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